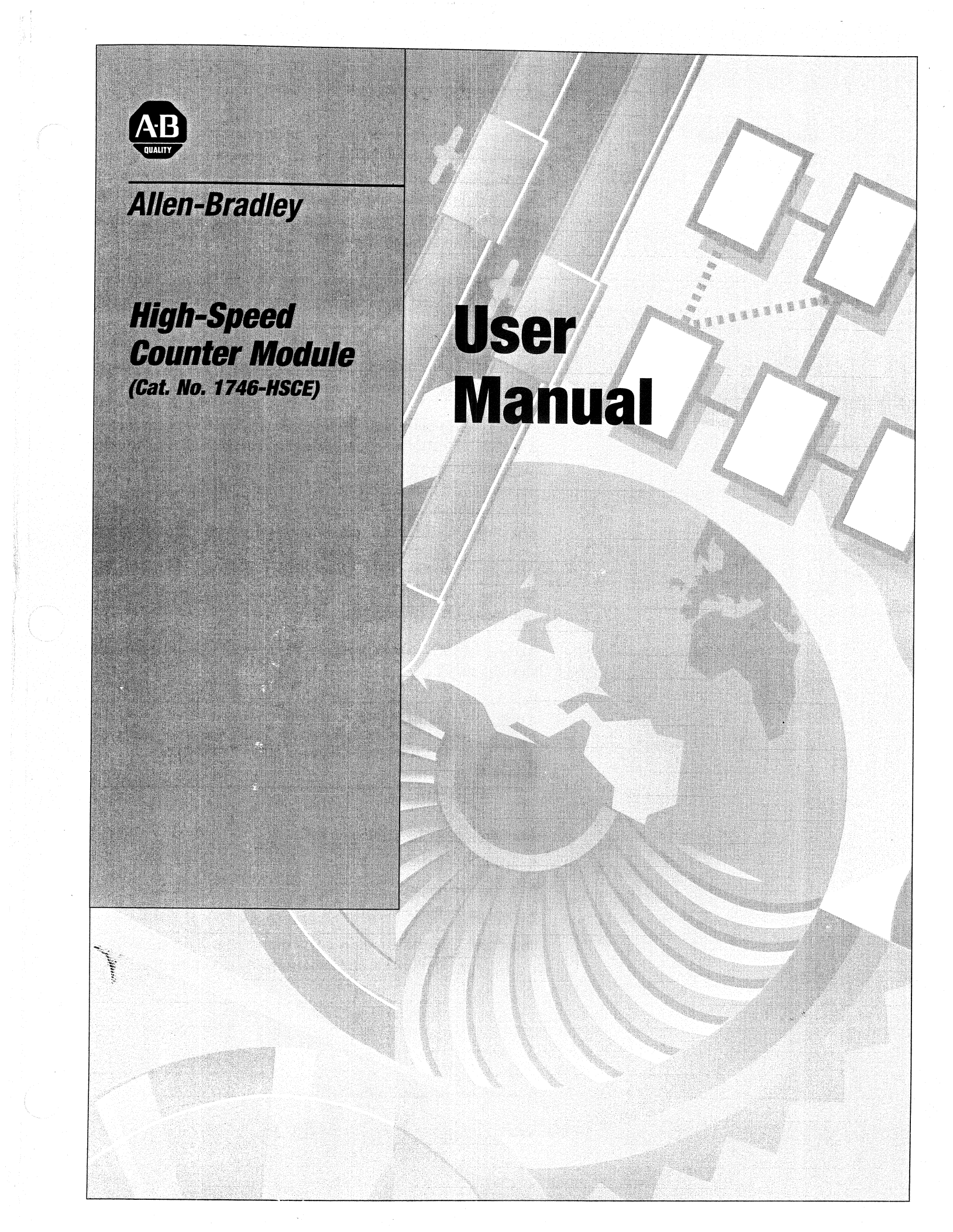

Allen-Bradley

High-Speed Counter Module

(Cat. No. 1746-HSCE)

User Manual

Important User Information

Because of the variety of uses for the products described in this publication, those responsible for the application and use of this control equipment must satisfy themselves that all necessary steps have been taken to assure that each application and use meets all performance and safety requirements, including any applicable laws, regulations, codes and standards.

The illustrations, charts, sample programs and layout examples shown in this guide are intended solely for purposes of example. Since there are many variables and requirements associated with any particular installation, Allen-Bradley does not assume responsibility or liability (to include intellectual property liability) for actual use based upon the examples shown in this publication.

Allen-Bradley publication SGI-1.1, *Safety Guidelines for the Application, Installation, and Maintenance of Solid-State Control* (available from your local Allen-Bradley office), describes some important differences between solid-state equipment and electromechanical devices that should be taken into consideration when applying products such as those described in this publication.

Throughout this manual we use notes to make you aware of safety considerations:

ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage or economic loss.

Attention statements help you to:

- identify a hazard
- avoid the hazard
- recognize the consequences

Important: Identifies information that is critical for successful application and understanding of the product.

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Summary of Changes

The information below summarizes the changes to this manual since the last printing as 1746–6.5 in January 1995.

To help you find new information and updated information in this release of the manual, we have included change bars as shown to the right of this paragraph.

New Information

The table below lists sections that document new features and additional information about existing features, and shows where to find this new information.

For This New Information	See
Terms and Abbreviations moved from Preface to Glossary	Glossary
The 1746-HSCE module is not compatible with the 1746-ASB module.	Chapter 1 – Module Overview
Output VDC must be user-supplied.	Chapter 1 – Module Overview Chapter 3 – Installation and Wiring
Compliance to European Union Directives statement.	Chapter 3 – Installation and Wiring Appendix A – Specifications
M file and G file information has been updated. I/O interrupt functionality of status bits has also been modified.	Appendix B – M0-M1 Files, G Files, and Interrupts

Installation and Wiring

Chapter 3

Configuration and Programming

Chapter 4

Start Up, Operation and Troubleshooting

Chapter 5

Application Examples

Chapter 6

Specifications

Appendix A

M0–M1 Files, G Files, and Interrupts

Appendix B

Differential Encoder Information

Appendix C

Special Considerations When Using APS Versions 2.01 and 3.01

Appendix D

Range/Rate Mode Configuration Worksheets

Appendix E

Sequencer Mode Configuration Worksheets

Appendix F

Glossary

Index

Preface

Read this preface to familiarize yourself with the rest of the manual. This preface covers the following topics:

- who should use this manual
- the purpose of this manual
- common techniques used in this manual
- Allen-Bradley support

Who Should Use this Manual

Use this manual if you are responsible for designing, installing, programming, or troubleshooting control systems that use Allen-Bradley small logic controllers.

You should have a basic understanding of SLC 500™ products. You should understand programmable controllers and be able to interpret the ladder logic instructions required to control your application. If you do not, contact your local Allen-Bradley representative for information on available training courses before using this product.

Purpose of this Manual

This manual is a reference guide for the High-Speed Counter Module. It describes the procedures you use to install, configure, and program the module for use with your SLC 5/02™ (or later) processor.

Contents of this Manual

Chapter	Title	Contents
	Preface	Describes the purpose, background, and scope of this manual. Also specifies the audience for whom this manual is intended.
1	Module Overview	Explains and illustrates the theory behind the High-Speed Counter's operation. Covers hardware and software features.
2	Module Operation	Describes input type selection, how the module uses various inputs and outputs, counter types, and operating modes.
3	Installation and Wiring	Provides dip switch and jumper settings, module installation, input and output connections, terminal block removal and wiring, and sample encoder and limit switch wiring diagrams.
4	Configuration and Programming	Provides the steps necessary to configure your SLC 5/02 (or above), specific M0, Input, and Output file information.
5	Start Up, Operation, and Troubleshooting	Describes startup information, normal operating states of the LEDs, troubleshooting, and error handling information.
6	Application Examples	Provides basic and supplementary examples which illustrate Sequencer, Range, and Rate mode operation.
Appendix A	Specifications	Lists specifications for temperature, humidity, input, output, voltage, timing, and cabling.
Appendix B	M0–M1 Files, G Files, and Interrupts	Provides M0, M1, G file, and Interrupt information.
Appendix C	Differential Encoder Information	Gives information on connecting a differential encoder.
Appendix D	Special Considerations When Using APS Versions 2.01 and 3.01	Provides procedures which must be followed if using versions 2.01 or 3.01 of APS with the High-Speed Counter module.
Appendix E	Range/Rate Mode Configuration Worksheets	Provides worksheets for the output and M0 file and the input data file.
Appendix F	Sequencer Mode Configuration Worksheets	Provides worksheets for the output and M0 file and the input data file.

Related Documentation

The following documents contain additional information concerning Allen-Bradley SLC™ products. To obtain a copy, contact your local Allen-Bradley office or distributor.

For	Read this Document	Document Number
An overview of the SLC 500 family of products	SLC 500 System Overview	1747-2.30
A description on how to install and use your *Modular* SLC 500 programmable controller	Installation & Operation Manual for Modular Hardware Style Programmable Controllers	1747-6.2
A procedural manual for technical personnel who use APS to develop control applications	Advanced Programming Software (APS) User Manual	9399-APSUM
A reference manual that contains status file data, instruction set, and troubleshooting information about APS	SLC 500™ and MicroLogix™ 1000 Instruction Set Reference Manual	1747-6.15
An introduction to APS for first-time users, containing basic concepts but focusing on simple tasks and exercises, and allowing the reader to begin programming in the shortest time possible	Advanced Programming Software Quick Start for New Users	9399-APSQS
A training and quick reference guide to APS	SLC 500 Software Programmer's Quick Reference Guide—available on PASSPORT at a list price of $50.00	ABT-1747-TSG001
A procedural and reference manual for technical personnel who use the APS import/export utility to convert APS files to ASCII and conversely ASCII to APS files	Advanced Programming Software Import/Export Utility User Manual	9399-APSIE
A procedural and reference manual for technical personnel who use an HHT to develop control applications	Allen-Bradley Hand-Held Terminal User Manual	1747-NP002
An introduction to HHT for first-time users, containing basic concepts but focusing on simple tasks and exercises, and allowing the reader to begin programming in the shortest time possible	Getting Started Guide for HHT	1747-NM009
In-depth information on grounding and wiring Allen-Bradley programmable controllers	Allen-Bradley Programmable Controller Grounding and Wiring Guidelines	1770-4.1
A description of important differences between solid-state programmable controller products and hard-wired electromechanical devices	Application Considerations for Solid-State Controls	SGI-1.1
An article on wire sizes and types for grounding electrical equipment	National Electrical Code	Published by the National Fire Protection Association of Boston, MA.
A complete listing of current Allen-Bradley documentation, including ordering instructions. Also indicates whether the documents are available on CD-ROM or in multi-languages.	Allen-Bradley Publication Index	SD499
A glossary of industrial automation terms and abbreviations	Allen-Bradley Industrial Automation Glossary	AG-7.1

Common Techniques Used in this Manual

The following conventions are used throughout this manual:

- Bulleted lists such as this one provide information, not procedural steps.
- Numbered lists provide sequential steps or hierarchical information.
- *Italic* type is used for emphasis.
- Text in `this font` indicates words or phrases you should type.

- Key names match the names shown and appear in bold, capital letters within brackets (for example, **[ENTER]**). A function key icon matches the name of the function key you should press, such as 

.

Allen-Bradley Support

Allen-Bradley offers support services worldwide, with over 75 Sales/Support Offices, 512 authorized Distributors and 260 authorized Systems Integrators located throughout the United States alone, plus Allen-Bradley representatives in every major country in the world.

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Contact your local Allen-Bradley representative for:

- sales and order support
- product technical training
- warranty support
- support service agreements

Technical Product Assistance

If you need to contact Allen-Bradley for technical assistance, please review the information in the Start Up, Operation, and Troubleshooting chapter first. Then call your local Allen-Bradley representative.

Your Questions or Comments on this Manual

If you find a problem with this manual, please notify us of it on the enclosed Publication Problem Report.

If you have any suggestions for how this manual could be made more useful to you, please contact us at the address below:

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Milwaukee, WI 53201-2086

Module Overview

This chapter contains the following:

- module overview
- operating modes
- hardware features

High-Speed Counter Module Overview

The High-Speed Counter Module, Catalog Number 1746-HSCE is an SLC 500 family compatible device. It can be used with SLC 5/02 (and above) processors.①

The module's bidirectional counting ability allows it to detect movement in either direction. In addition, x2 and x4 counting modes are provided to fully use the capabilities of high resolution quadrature encoders.

High-speed inputs from quadrature encoders and various high-speed switches are supported. Accepting input pulse frequencies of up to 50k Hz allows precise control of fast motions.

In addition to providing an Accumulated Counter, the module provides a Rate Counter to determine Rate Measurement by indicating the pulse input frequency in Hz. (Refer to the block diagram on the following page.) The Rate Measurement is determined by accumulating input pulses over a fixed period of time. You set the Rate Period to best match your application requirements.

Background Rate calculation is provided in Sequencer and Range Modes. This operation accepts input rates up to 32,767 Hz. The dynamically configurable Rate Period ranges from 10 ms to 2.55 seconds.

The module's four current sink (open collector) outputs can be controlled from one of two sources:

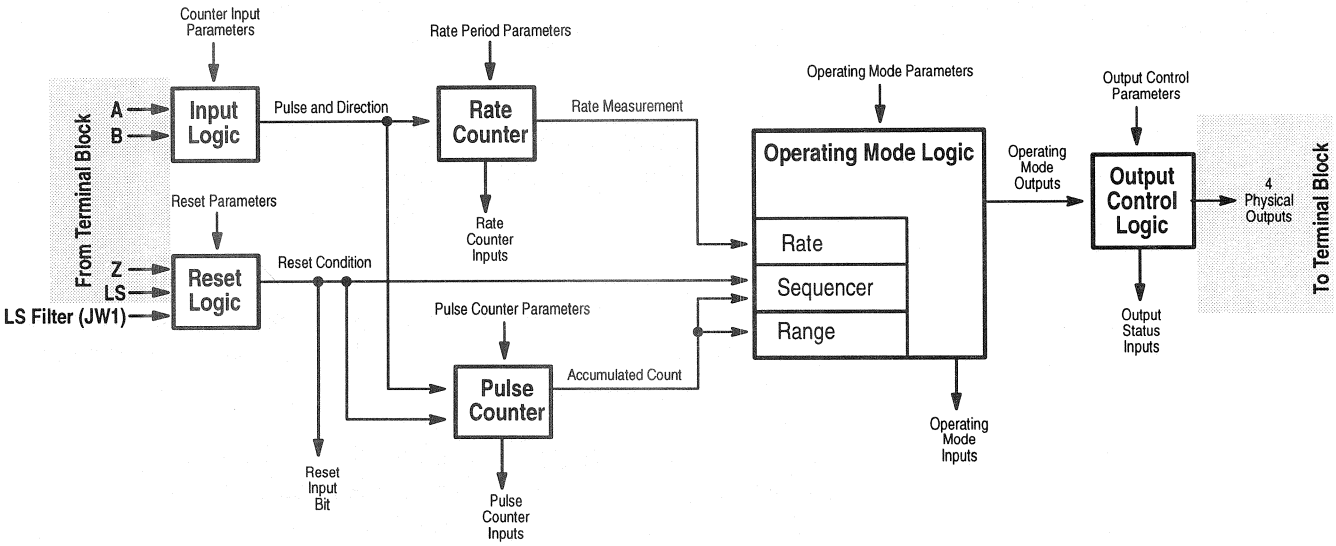
- the user program
- the module

Control of the counter reset is configured through user-set parameters. The counter can be reset from any combination of the Z input, Limit Switch input, or Soft Reset control bits.

① The 1746-NT4 Thermocouple Module is not compatible with the 1747-ASB Remote I/O Adapter Module.

Module operation is determined by selections made in the Setup and Control Word (M0:e.1). Setting the Function Control bit to 1 triggers the module to start the proper pulse counter, rate measurement, and output control functions. Many parameters are dynamic and can be changed without disrupting counter operation.

A block diagram of the module is shown below. Inputs from the terminal block enter the diagram at the left, outputs to the terminal block exit at the right. M0 and Output file parameters from the SLC enter the logic blocks from the top. Input file data to the SLC exit the logic blocks from the bottom.



Counter Input Parameters
- Input Type (M0:e.1/9–11)
- Up/Down Count Direction (M0:e.1/3) *–d*

Reset Parameters
- Soft Reset bit (M0:e.1/4) *–d*
- Reset Mode (M0:e.1/5–7)

Rate Period Parameters
- Rate Period (M0:e.9/0–7 or M0:e.16/0–7) *–d*

Operating Mode Parameters
- Operating Mode (M0:e.1/14–15)
- Function Control Bit (M0:e.1/12)
- Range Definitions:
  - Range Starting Values (M0:e.10 – 33) *–d*
  - Range Ending Values (M0:e.10 – 33) *–d*
  - Range Outputs (M0:e.3 – 8) *–d*
  - Valid Ranges (M0:e.2) *–d*
- Sequencer Definitions:
  - Valid Steps (M0:e.2 and M0:e.3/0–7) *–d*
  - Step Presets (M0:e.17 – 40) *–d*
  - Step Outputs (M0:e.4 – 15) *–d*
  - Initial Outputs (M0:e.3/8–15) *–d*
  - Sequencer Reset (M0:e.1/0) *–d*

Pulse Counter Parameters
- Reset Value (M0:e.34 or M0:e.41) *–d*
- Maximum Count Value (M0:e.34 or M0:e.41)
- Counter Hold bit (M0:e.1/2) *–d*
- Counter Type bit (M0:e.1/13)

Output Control Parameters
- Direct Outputs (O:e.0/0–7) *–d*
- Output Source Select (M0:e.0/0–7) *–d*
- Enable Outputs bit (M0:e.1/1) *–d*

Rate Counter Inputs
- Rate Valid (I:e.0/3)
- Rate Counter Overflow (I:e.0/4)
- Rate Measurement Overflow (I:e.0/5)
- Zero Rate Period Count (I:e.0/2)
- Rate Period Count (I:e.2)
- Rate Measurement (I:e.3)

Pulse Counter Inputs
- Accumulated Count (I:e.1)
- Overflow/Underflow (I:e.0/13)
- Pulse Counter State (I:e.0/14–15)

Reset Input bit (I:e.0/12)

Operating Mode Inputs
- Sequencer Inputs
  - Current Sequencer Step (I:e.5/0–7)
  - Next Sequencer Step (I:e.5/8–15)
  - Sequence Done (I:e.0/6)
- Range inputs
  - Ranges Active (I:e.6/0–11)

Output Status Inputs (I:e.4/8–15)

Error Inputs
- Critical Error (I:e.0/10)
- Configuration Error bit (I:e.0/11)
- Configuration Error Code (I:e.4/0–7)

–d indicates a dynamic parameter

Operating Modes

The module operates in 3 modes: Range, Rate, and Sequencer. Specific operating mode information is contained in chapter 2, Module Operation. The following information summarizes the module's operating modes.

Important: Appendixes E and F contain blank worksheets to assist you when configuring your module. Appendix E contains worksheets for Range and Rate Mode operation. Appendix F contains worksheets for the Sequencer Mode operation.

Range Mode

In the Range Mode, you define a group of count ranges and define the outputs to be active when the Accumulated Count value is within each range. In this mode, the module offers:

- up to 12 ranges
- dynamically configurable ranges
- ring or linear counter operation
- input rate calculation
- direct SLC processor control of unused outputs

Rate Mode

In the Rate Mode, you define a group of rate ranges and corresponding outputs. When the Rate Measurement is within each defined range, the corresponding outputs are active. In this mode, the module offers:

- Rate Periods from 10 ms to 2.55 seconds
- input rates up to 32,767 Hz in either direction
- up to 12 ranges
- ring or linear counter operation
- dynamically configurable Rate Period and range values

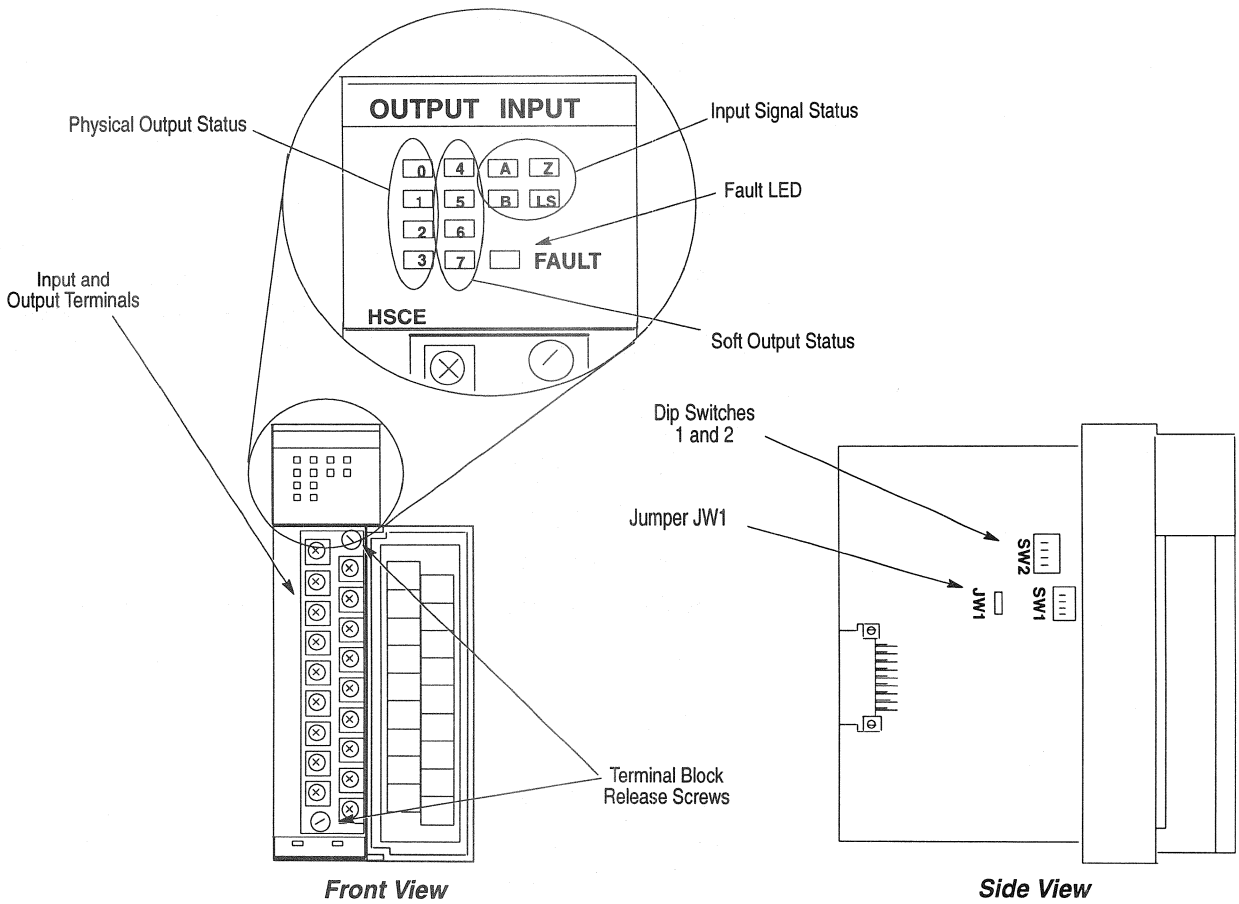
Sequencer Mode

In the Sequencer Mode, you define a sequence of presets and a series of corresponding output patterns. When the Accumulated Count passes the next preset, the outputs are updated to the corresponding pattern. In this mode, the module offers:

- up to 24 discrete steps
- dynamically configurable steps
- automatic restart at the end of each sequence
- external sequence reset control
- ring or linear counter operation
- input rate calculation
- direct SLC processor control of unused outputs

Hardware Features

The features of the module are highlighted below. Detailed installation and wiring instructions are contained in chapter 3.



LEDs

These LEDs illuminate when their corresponding input or output is active:

- LEDs 0 – 3 correspond to Physical Outputs 0 – 3.
- LEDs 4 – 7 correspond to Soft Outputs 4 – 7.
- LEDs A, B, Z, and LS indicate the input is energized.
- LED FAULT illuminates when the module is faulted.

Input and Output Terminals

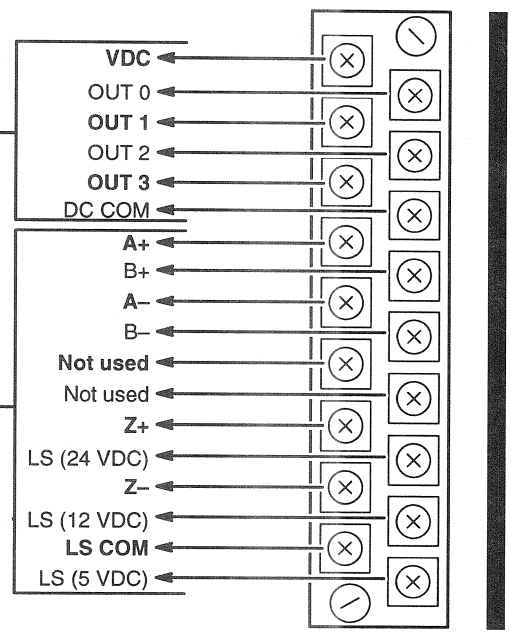
These terminals supply power and inputs to the module and outputs to the attached output devices. They can accommodate two 14 AWG wires. A wiring diagram and templates are located in chapter 3.

Discrete Output Wiring

NOTE: VDC must be externally supplied by the user. See page 3–8 for output wiring.

Limit Switch and Encoder Input Wiring

See pages 3–11 through 3–15 for input wiring.



Dip Switches 1 and 2

- SW1 selects the type of input, single ended or differential.
- SW2 selects the output voltage of 4.5–10V dc or 10–30V dc.

See chapter 3 for default switch settings.

Jumper JW1

JW1 selects the filtering rate used to debounce the limit switch input. Filtering rates are 300 µs and 10 ms.

See chapter 3 for default jumper setting.

Module Operation

This chapter describes the basic operation of the module. Specific programming information and individual memory maps for each mode are contained in chapter 4. This chapter contains overviews of:

- module overview
- input type selection
- pulse and direction input
- quadrature encoder input
- up/down pulse input
- the input pulse counter
- the rate measurement calculation
- output control
- range, rate, and sequencer modes

Module Overview

The main function of the module is to count the input pulses that occur on the input channels A and B. Counter control and reset control is provided through user configuration parameters. The counter can be reset from any combination of the Z input, LS (limit switch) input, and Soft Reset control bit.

In addition to the Accumulated Count, the module provides the Rate Measurement indicating the pulse input frequency in Hz. The Rate Measurement is determined by accumulating input pulses over a fixed period of time. You set the rate period to best match your application requirements.

The module's four current sink (open collector) outputs can be controlled from one of two sources:

- the user program (in the Direct Outputs field)
- the module:
  - when the Accumulated Count is within user specified ranges in Range Mode
  - when the Accumulated Count passes specified preset values in Sequencer Mode
  - when the Rate Measurement is within user specified ranges in Rate Mode

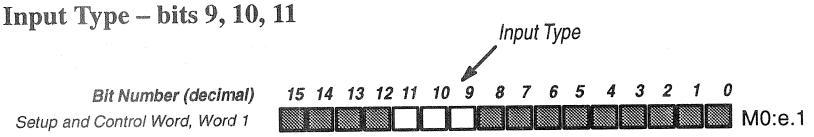
The above sources are determined by the Operating Mode and the Output Source Select fields.

Module operation is determined by user-defined configuration parameters. Setting the Function Control bit to 1 starts the proper pulse counter, Rate Measurement, and output control functions. Dynamic parameters can be changed regardless of the Function Control bit. Static Parameters can be changed only when the Function Control bit is reset (to 0).

Input Type Selection

The type of input you require for your application is selected by means of three bits located in the Setup and Control Word (M0:e.1). The table below indicates how the bits must be set to configure quadrature encoder, pulse and direction, or up/down pulse inputs.

Input Type – bits 9, 10, 11



Setup and Control Word Bits			Input Type
11	10	9	
0	0	0	Invalid – configuration error
0	0	1	Invalid – configuration error
0	1	0	Pulse and Direction w/External Control
0	1	1	Pulse and Direction w/Internal Control
1	0	0	Quadrature Encoder Input – X1
1	0	1	Quadrature Encoder Input – X2
1	1	0	Quadrature Encoder Input – X4
1	1	1	Up/Down Pulse Inputs

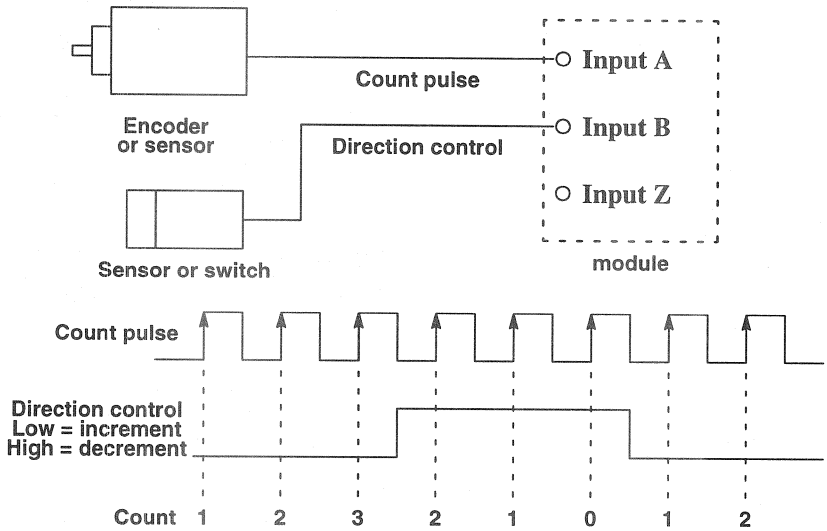
The input type you select determines how the A and B inputs cause the module's counter to increment and decrement. For all three input types, the Z input can be used to force a counter reset. The A, B, and Z inputs operate with input signals up to a maximum rate of 50k Hz.

Pulse and Direction Input

In this configuration, count pulses are applied to input A. The counter direction is controlled by either the Up/Down Count Direction bit, or by an external signal applied to input B (depending on the selection made in M0:e.1/9–11).

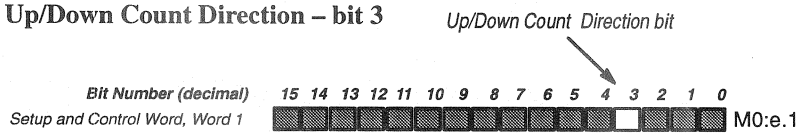
When Pulse and Direction with External Control is chosen, the B input controls the direction (as illustrated below). If input B is low, the counter increments on the rising edges of input A. If input B is high, the counter decrements on the rising edges of input A.

Important: Specific wiring information is contained in Chapter 3.



The count direction can be controlled from your user program rather than using a control signal connected to input B. This can be accomplished with the Up/Down Count Direction bit (M0:e.1/3) as follows:

Up/Down Count Direction – bit 3



Setup and Control Word, Bit 3	Affect on Accumulated Count
1	Accumulated Count decrements with each count received on Input A
0	Accumulated Count increments with each count received on Input A

Important: When internally controlling the direction with the Up/Down Count Direction bit, input B has no affect.

When externally controlling the direction with Input B, the Up/Down Count Direction bit (M0:e.1/3) has no affect.

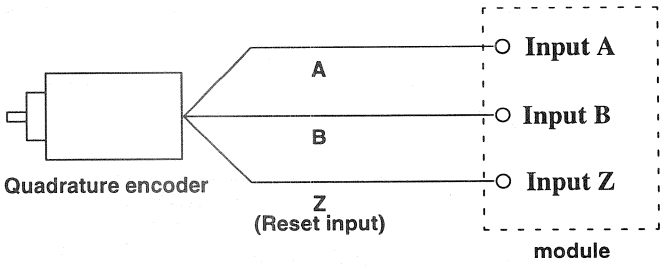
Quadrature Encoder Input

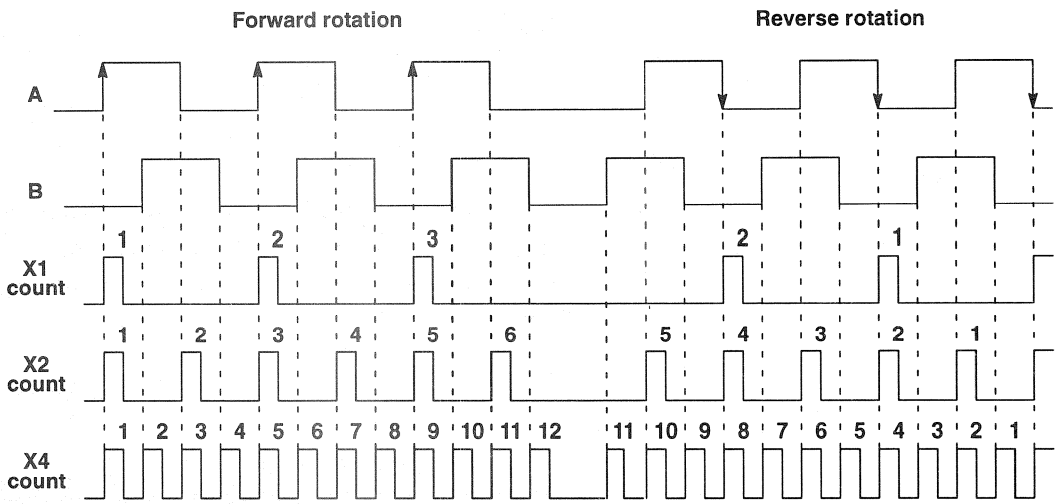
The figure below shows a quadrature encoder connected to inputs A, B, and Z. The count direction is determined by the phase angle between input A and input B. If A leads B, the counter increments. If B leads A, the counter decrements.

The counter resolution can be selected so that the count increments/decrements on one edge of input A only (X1), on both edges of input A (X2), or on both edges of input A and input B (X4).

The counter can be reset using the Z input, as described in *Counter Reset Control* on page 2–7.

Important: The connection of A, B, and Z is critical, refer to chapter 3 and appendix C.



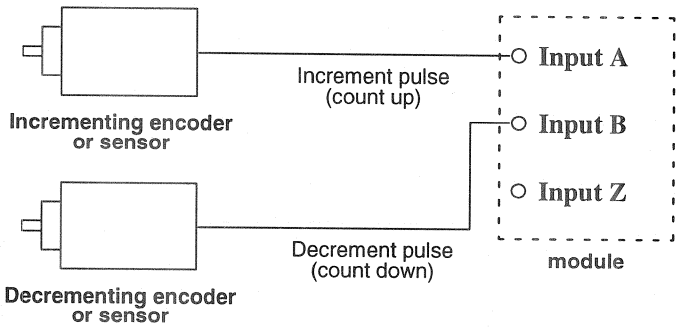


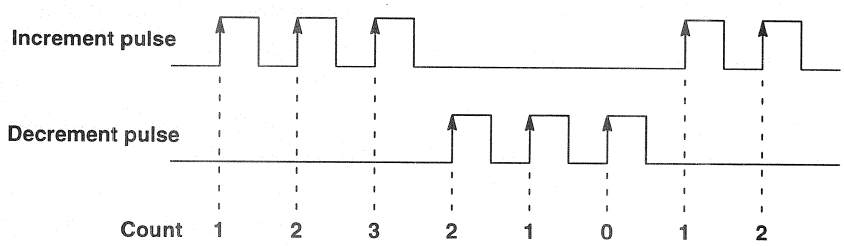
Up/Down Pulse Inputs

With this input type, the counter increments on the rising edge of pulses applied to input A and decrements on the rising edge of pulses applied to input B. If pulses are applied to inputs A and B simultaneously, the pulse counter retains its previous value.

The counter can be reset as described in *Counter Reset Control* on page 2–7.

Important: Specific wiring information is contained in chapter 3.





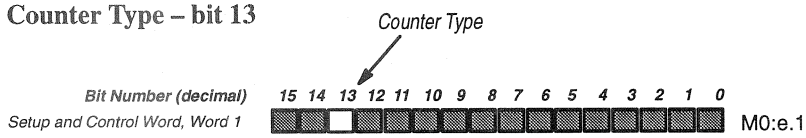
Input Pulse Counter

The module's input pulse counter has the ability to count input pulses at a rate of up to 50k Hz. Several types of channel A and B input configurations are supported as discussed previously. The resulting Accumulated Count value is available in the module's Input Data File.

Counter Types

The module provides two types of counter operation, ring and linear. The selection is made by the Counter Type bit (M0:e.1/13) as follows:

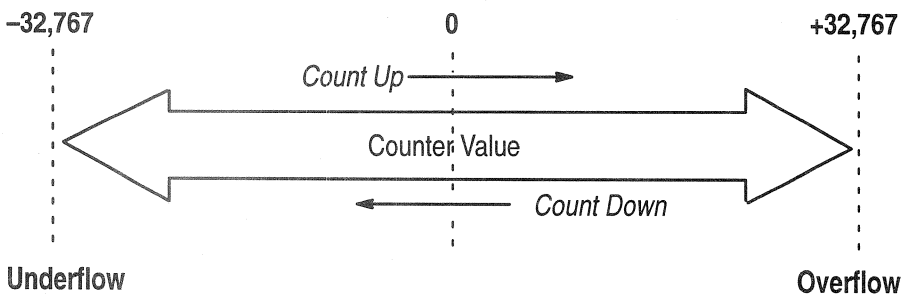
Counter Type – bit 13



Counter Type Bit (bit 13)	Counter Type
0	Linear
1	Ring

Linear Counter

The figure below demonstrates linear counter operation. In linear operation the count value must remain in the range of –32767 to +32767. If the count value goes above +32767 or below –32767, a linear counter overflow/underflow error results. This condition is indicated by a 1 in the Over/Underflow bit (I:e.0/13). This is a critical error that halts operation of the module. Refer to *Linear Counter Overflow* located in chapter 5.



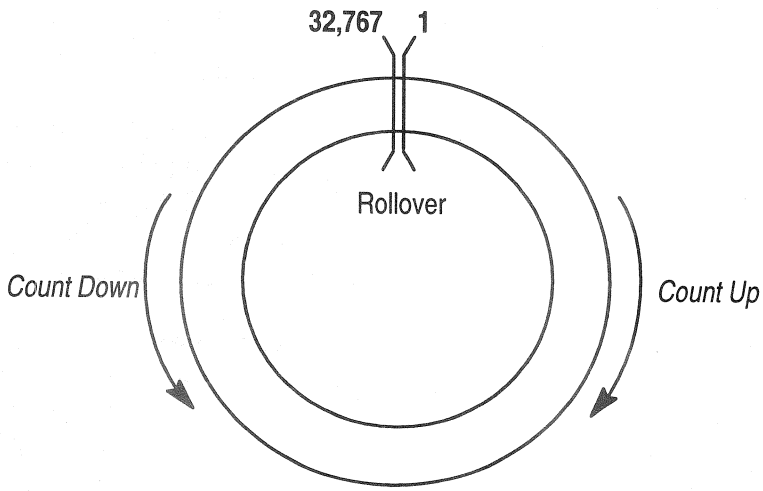
The linear counter can be configured to reset to a nonzero value through the reset parameter.

Important: If the reset value is nonzero, there is a delay of up to 500 µs before the reset value is loaded. Count pulses can be lost if they happen during the delay time. Refer to *Timing Information* in appendix A.

Ring Counter

The figure below demonstrates ring counter operation. In ring counter operation, the count value goes between 0 and a maximum value. The maximum value must be entered in the Maximum Count Value (M0:e.34 Range and Rate Mode, M0:e.41 Sequencer Mode).

The ring counter automatically rolls over to 0 if the count exceeds the maximum value. If the count goes below 0 it rolls over to the maximum value. The ring counter always resets to zero.



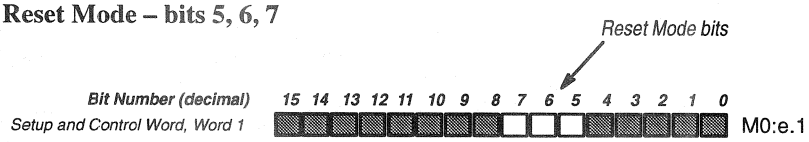
Counter Reset Control

Reset Mode (bits 5,6,7) allows you to select the Accumulated Counter reset conditions. If the pulse counter is reset, the rate calculation is not affected. Bit 5 enables the Z reset, Bit 6 enables the limit switch reset, and bit 7 enables the Soft Reset. The counter can be reset from any combination of the Z input, LS input, or Soft Reset bit (M0:e.1/4).

In the Sequencer Mode, you can reset the sequencer to the Initial Output pattern (M0:e.3/8–15) using the Sequencer Reset bit (M0:e.1/0).

The three bits can be set as follows:

Reset Mode – bits 5, 6, 7



Setup and Control Word Bits			Reset Condition is True
7	6	5	
0	0	0	Never
0	0	1	When Z is ON
0	1	0	When the limit switch is ON
0	1	1	When the limit switch and Z are ON
1	0	0	When the Soft Reset is 1
1	0	1	When the Soft Reset is 1 and Z is ON
1	1	0	When the Soft Reset is 1 and limit switch is ON
1	1	1	When the Soft Reset is 1, limit switch and Z are ON

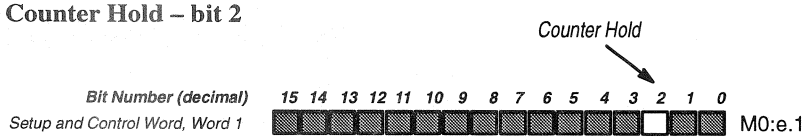
The reset of the counter is edge triggered. It occurs only when all of the conditions specified become true. If multiple conditions are selected, the counter is reset on the last event's 0 to 1 transition. For example, if Z and LS are selected (011), Z by itself will not trigger the reset. Z and LS must both be ON.

Important: The time it takes for the counter to reset depends upon the value it resets to. If the reset value is zero, the counter resets immediately on the false to true edge of the reset condition without losing subsequent counts. If the reset value is nonzero, there is a delay of up to 500 µs before the reset value is loaded. Count pulses can be lost if they happen during the delay time. Refer to *Timing Information* in appendix A.

Counter Hold Control

The pulse counter value is held when the user program sets the Counter Hold bit (M0:e.1/2) to 1. When this bit is set, the Accumulated Count does not change when input pulses occur. However, the counter reset is still active. The pulse counter's Accumulated Count is reset when a reset is received while the counter is held (Counter Hold =1).

Counter Hold – bit 2



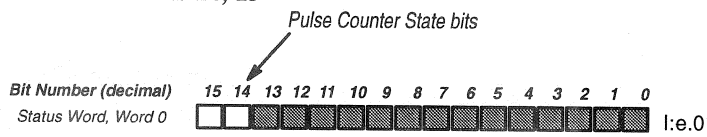
Counter Hold (bit 2)	Counter State
0	counter is running
1	count is held

Pulse Counter State

When the SLC processor enters run or test mode, the Accumulated Count is reset to 0. It is held at 0 until the user program completes module configuration and the Function Control bit is set to 1. If the Function Control bit is reset to 0, the counter will again be reset and held at 0 until the Function Control bit returns to 1.

The counter state is available to the user program in the Pulse Counter State field (I:e.0/14–15). This field is defined as follows:

Pulse Counter State – bits 14, 15



Status Word Bits		Pulse Counter State
15	14	
0	0	stopped
0	1	running
1	0	undefined
1	1	hold

Rate Measurement

Using the Rate Counter, the module measures the frequency of the input pulses in the range of –32767 Hz to 32767 Hz. The resulting value is available in the Rate Measurement word (I:e.3). The number of pulses counted in the interval is made available in the Rate Period Count word (I:e.2).

Important: If the input pulse rate is above 32,767 Hz, a Rate Measurement Overflow occurs. The Rate Measurement Overflow bit (I:e.0/5) will then be set to 1. Refer to *Rate Measurement Overflow* located in chapter 5.

Rate Measurement Calculation

The module calculates the Rate Measurement by counting pulses in a fixed interval of time. You enter the fixed interval in the Rate Period parameter. This value is set in increments of 10 ms, from 10 ms to 2.55 seconds. The number of pulses counted in the interval is made available in the Rate Period Count word (I:e.2). Pulses increment or decrement the count. For example, if 8 up counts and 9 down counts are received in one Rate Period, the Rate Period Count will be equal to –1.

If the Input type has been selected as X2 or X4 encoder, the Rate Period Count is counted on both edges of A or both edges of A and B respectively.

The resulting Rate Measurement is determined by dividing the Rate Period Count by the Rate Period and by dividing out the X2 or X4 encoder multiplier:

Rate Measurement = Rate Period Count / Rate Period

for X2 encoder:

Rate Measurement = (Rate Period Count / Rate Period)/2

for X4 encoder:

Rate Measurement = (Rate Period Count / Rate Period)/4

The Rate Period Count can have values between –32767 and 32767. If more than 32767 counts arrive in the Rate Period, the Rate Counter Overflow bit (I:e.0/4) is set to 1. Refer to *Rate Counter Overflow* located in chapter 5.

If the Rate Measurement value is valid (a rate sample was taken and no Rate Counter Overflow and no Rate Measurement Overflow occurred) the Rate Valid bit (I:e.0/3) is set. This bit can be monitored by the user program to insure a valid rate value is available.

If no pulses were counted during the Rate Period, the Zero Rate Period Count bit (I:e.0/2) is set.

Selecting the Rate Period Parameter

The Rate Period parameter defaults to 0 and must be set to a value between 1 and 255 (10 ms to 2.55 seconds) to avoid a configuration error. Consider the following when selecting the Rate Period:

- Make sure your Rate Period does not allow a Rate Counter Overflow to occur. This will depend on the maximum pulse frequency and input type. For example if the maximum input frequency is 10k Hz and the input type is X2 encoder:

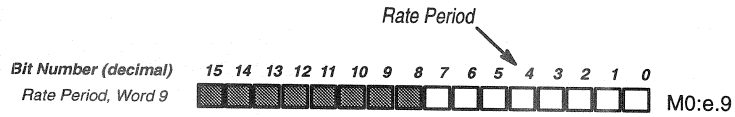
  Rate Period < 32767/(10000 x 2) = 1.63 seconds

  The Rate Period should be set less than 1.63 seconds for this example.
- A large Rate Period will introduce a delay in system response to a rate change. If system response is critical keep the Rate Period short. However, if system response is not critical, a longer Rate Period will help filter the Rate Period measurement.
- The shorter the Rate Period, the less accurate the resulting Rate Measurement. The maximum error of the measurement can be expressed as:

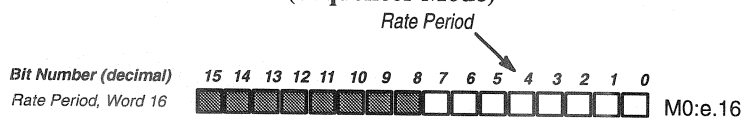
  Maximum Error = 1/Rate Period

For example, if the Rate Period = .5 seconds, the resulting Rate Measurement is accurate to within 2 Hz.

Rate Period – bits 0 to 7 (Range and Rate Mode)



Rate Period – bits 0 to 7 (Sequencer Mode)



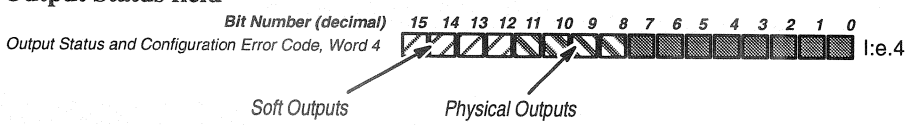
Output Control

Physical and Soft Outputs

The module provides 4 physical outputs. You select whether these outputs are to be activated from the user program or from the module in response to specified input events (refer to Output Source Select M0:e.0/0–7). The states of these 4 Physical Outputs are available to the user program in the Output Status field (I:e.4/8–11).

In addition to the Physical Outputs, 4 Soft Outputs are available. Soft Outputs appear in the Outputs Status field (I:e.4/12–15). They do not have a physical output associated with them, but can be used as event flags in the user program.

Output Status field

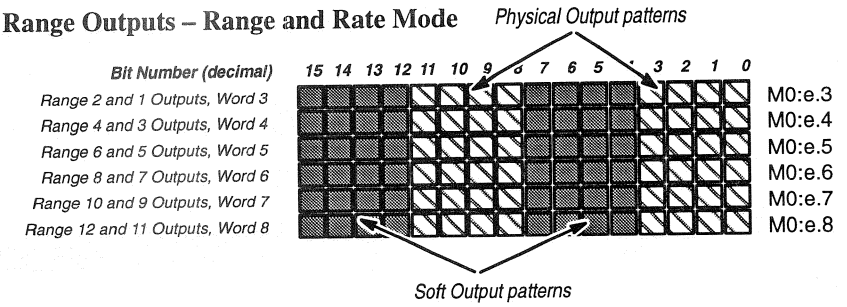


The Range Outputs (Range and Rate Mode) and Step Outputs (Sequencer Mode) fields contain the output patterns that are applied to the Physical and Soft Outputs.

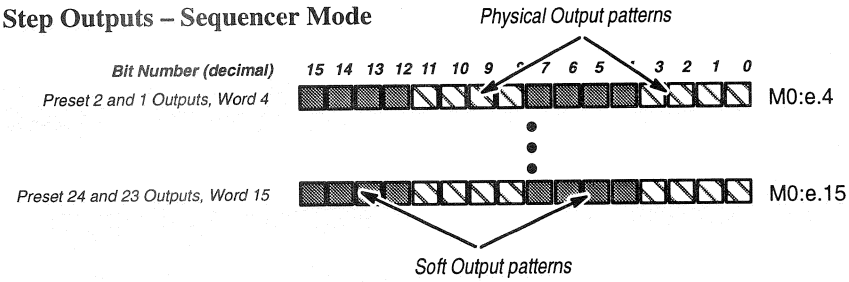
When the count is within a Valid Range (Range and Rate Mode), or Valid Step (Sequencer Mode), the corresponding output pattern is applied to the Output Status field (I:e.4/8–15) and the modules output terminals.

For example, in Range Mode, when the count is within Range 2, the Range 2 Outputs field is applied to the Output Status field (I:e.4/8–15) and output terminals.

Range Outputs – Range and Rate Mode



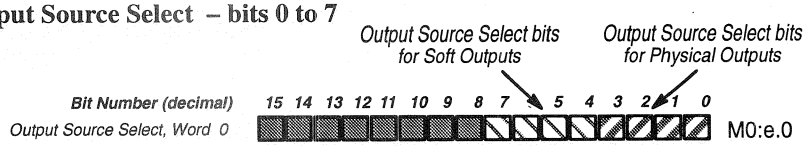
Step Outputs – Sequencer Mode



Output Source Select

The Output Source Select (M0:e.0/0–7) is used to specify whether the outputs are activated by the user program or from the module. Each bit represents an output. When set to 1, the associated output is controlled by the user program. When an Output Source Select bit is set to 1, the user program can set a bit in the Direct Output field (O:e.0/0–7) which turns an output ON.

Output Source Select – bits 0 to 7



Output Start Up and Enabling

When the SLC processor is *not* in run mode, the module outputs are disabled. After the SLC processor enters run mode, the module examines the Direct Output fields (O:e.0/0–7).

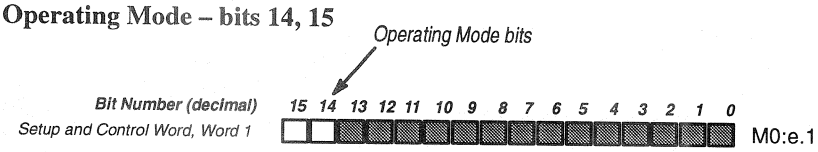
All outputs under module control are disabled until after the module configuration has been completed and the Function Control bit has been set to 1. If the Function Control bit is returned to 0 the module controlled outputs will again be disabled. The user program controlled outputs are not affected by the Function Control bit.

When reset to 0, the Enable Outputs bit (M0:e.1/1) disables module and user program controlled outputs.

Operating Mode

The Operating Mode field (M0:e.1/14–15) is used to select the module's mode of operation. The field is specified as follows:

Operating Mode – bits 14, 15



Operating Mode Bits		Output Operating Mode
15	14	
0	0	invalid
0	1	Range
1	0	Sequencer
1	1	Rate

Important: Appendixes E and F contain blank worksheets to assist you when configuring your module. Appendix E contains worksheets for Range and Rate Mode operation. Appendix F contains worksheets for the Sequencer Mode operation.

Range Mode

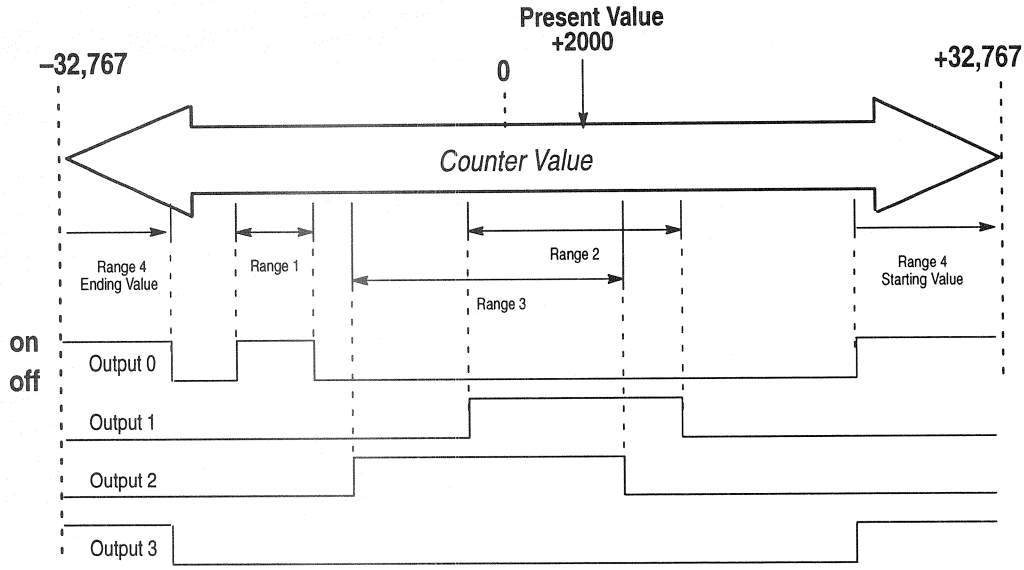
In the Range Mode, you use the counter ranges to specify the outputs to be active within each range. Ranges may overlap. The ranges are defined using the Starting and Ending Values (M0:e.10 – 33).

The Range Outputs fields (M0:e.3 – 8) contain the output patterns that specify which outputs are active. Output patterns are applied to the Output Status field (I:e.4/8–15) and output terminals when the count is within the associated range (*i.e.* while in Range 2, the Range 2 Outputs are applied). When the count is within more than one range, the output patterns of those ranges are combined (logically ORed).

Ranges are enabled using the Valid Ranges field (M0:e.2). The ranges that are currently active are shown in the Ranges Active field (I:e.6/0–11). Each range has a corresponding bit location. A 1 indicates the Accumulated Count is within the range.

Shown below is the Range Mode when a linear counter is used. Note that Range 4 has an Ending Value that is less than the Starting Value.

Range Mode with Linear Counter



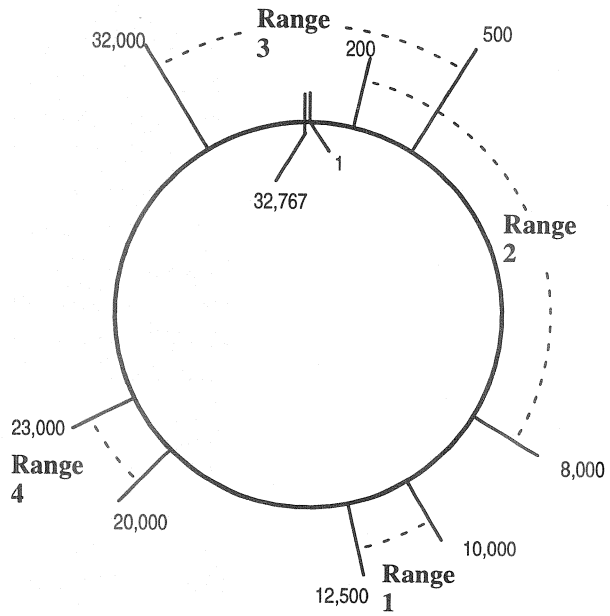
Range	Starting Value	Ending Value	Outputs ① 7	6	5	4	3	2	1	0	Outputs On
1	–7000	–5000	0	0	0	0	0	0	0	1	0
2	–1000	+4500	0	0	0	0	0	0	1	0	1
3	–4000	+3000	0	0	0	0	0	1	0	0	2
4	+9000	–9000	0	0	0	0	1	0	0	1	0 and 3

① Bits 0 – 3 are Physical Outputs. Bits 4 – 7 are Soft Outputs.

In this example, four ranges are specified. Configuration data for the counter is shown in the table. It indicates that output 0 is on for counts within range 1, output 1 is on for counts within range 2, output 2 is on for counts within range 3, and both outputs 0 and 3 are on for counts within range 4. When the count is 2000, outputs 2 and 1 are on, since 2000 falls within ranges 2 and 3.

The figure below demonstrates Range Mode when a ring counter is used.

Range Mode with Ring Counter



Range	Starting Value	Ending Value	Outputs ① 7	6	5	4	3	2	1	0	Outputs On
1	10,000	12,500	0	0	0	0	0	0	0	1	0
2	200	8,000	0	0	0	0	0	0	1	0	1
3	32,000	500	0	0	0	0	0	1	0	0	2
4	20,000	23,000	0	0	0	0	1	0	0	1	0 and 3

① Bits 0 – 3 are Physical Outputs. Bits 4 – 7 are Soft Outputs.

In the Range Mode, you use the counter ranges to specify the outputs to be active within each range. Ranges may overlap. The ranges are defined using the Starting and Ending Values (M0:e.10 – 33).

The Range Outputs fields (M0:e.3 – 8) contain the output patterns that specify which outputs are active. Output patterns are applied to the Output Status field (I:e.4/8–15) and output terminals when the count is within the associated range (*e.g.,* while in Range 2, the Range 2 Outputs are applied). When the count is within more than one range, the output patterns of those ranges are combined (logically ORed). Ranges are enabled using the Valid Ranges field (M0:e.2).

The ranges that are currently active are shown in the Ranges Active word (I:e.6). Each range has a corresponding bit location. A 1 indicates the Accumulated Count is within the range.

Rate Mode

The Rate Mode operates much the same as the Range Mode except the ranges are defined by the Rate Measurement value instead of the Accumulated Count value. Ranges may overlap.

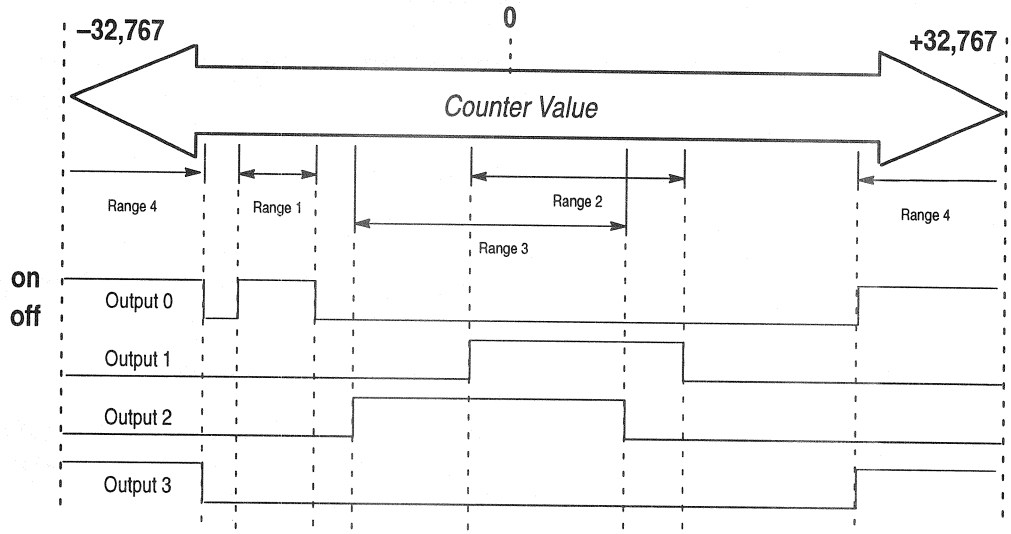
The 12 ranges are defined using the Starting and Ending Values (M0:e.10 – 33). The Range Outputs fields (M0:e.3 – 8) contain the output patterns that specify which outputs are active. Output patterns are applied to the Output Status field (I:e.4/8–15) and output terminals when the rate is within the associated range. When the rate is within more than one range, the output patterns are combined (logically ORed). Ranges are enabled using the Valid Ranges field (M0:e.2). The ranges that are currently active are shown in the Ranges Active word (I:e.6). Each range has a corresponding bit location. A 1 indicates the Rate Measurement is within the range.

When using Rate Mode, use the Ring Counter and set the Reset Value/Maximum Count Value (M0:e.34)) to 32,767. Doing so allows the counter to roll over after reaching 32,767. If the Linear Counter counts beyond 32,767, it will cause an overflow (as explained in *Linear Counter Overflow*, found in chapter 5).

Important: Appendix E contains blank worksheets to assist you when configuring your module for Rate Mode operation.

ATTENTION: If the input pulse rate is above 32767 Hz, a Rate Measurement Overflow occurs. The Rate Measurement Overflow bit (I:e.0/5) will then be set to 1. Refer to *Rate Measurement Overflow*, found in chapter 5.

Rate Mode with Linear Counter



Range	Starting Value	Ending Value	Outputs ① 7	6	5	4	3	2	1	0	Outputs On
1	–7000 Hz	–5000 Hz	0	0	0	0	0	0	0	1	0
2	–1000 Hz	+4500 Hz	0	0	0	0	0	0	1	0	1
3	–4000 Hz	+3000 Hz	0	0	0	0	0	1	0	0	2
4	+20,000 Hz	–20,000 Hz	0	0	0	0	1	0	0	1	0 and 3

① Bits 0 – 3 are Physical Outputs. Bits 4 – 7 are Soft Outputs.

Sequencer Mode

Use this mode when a repeatable sequence of events is required. This mode allows you to program a sequence of up to 24 steps.

Configuration

To define a step, you:

- set a bit in the *Valid Steps* field which corresponds to the step
- program the *Step Preset* value
- program the *Step Output* value

Important: Appendix F contains blank worksheets to assist you when configuring your module for Sequencer Mode operation.

The **Valid Steps** (M0:e.2 to M0:e.3/0–7) define which of the 24 possible steps are being used in the sequence. The bits in M0:e.2 through M0:e.3/0–7 represent steps 1 through 24. When a bit is set to 1, the corresponding step is enabled (part of the sequence). If a bit is reset to 0, the corresponding step is disabled (not part of the sequence).

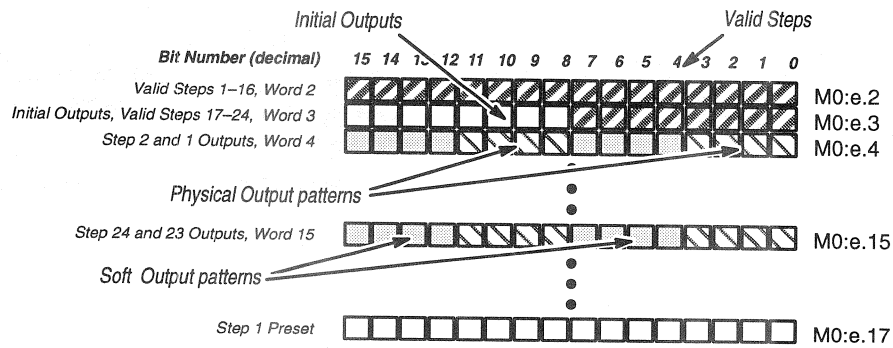
Each of the **Step 1 – 24 Preset** (M0:e.17 – 40) values has an associated preset value. The Step 1 – 24 Preset values define the number of pulses required to reach the corresponding step (the step is reached at one count beyond the preset). This value refers to the Accumulated Count value, not the relative number of pulses received between steps.

Each of the **Step 1 – 24 Output** values (M0:e.4 – 15) has an associated output value. The Step 1 – 24 Output values define the output pattern applied to the Physical and Soft Outputs when the associated step is reached.

The Initial Output (M0:e.3/8–15) is applied to the Physical and Soft Outputs only when the sequencer is initialized. Initialization occurs when the Function Control bit (M0:e.1/12) is toggled from 0 to 1, or when a pulse counter reset occurs and the Sequencer Reset bit (M0:e.1/0) is set to 1.

Important: Although the Valid Steps can be dynamically changed by adding or removing steps while the Function Control bit (M0:e.1/12) is set to 1 (sequencer is running), it should only be done by experienced programmers. The disabling or enabling of steps above the current step while the Function Control bit (M0:e.1/12) is set may not take effect until the next pass through the sequence. To assure the proper sequence, a step should not be enabled or disabled while the Function Control bit (M0:e.1/12) is set to 1.

Initial Outputs, Step Outputs, Valid Steps, and Step Presets



Sequencer Mode Operation

A step is reached on the next count after the Accumulated Count matches the Step Preset value. When a step is reached, the Step Output value for that step is applied to the Physical and Soft Outputs.

When the sequencer is first enabled (or reset), the Initial Output pattern (M0:e.3/8–15) is applied to the Physical and Soft Outputs. The module then proceeds through each step in the sequence in ascending order (1 – 24), as defined in the Valid Steps field (M0:e.2 to M0:e.3/0–7).

After the sequencer has reached the last Valid Step, it wraps around to the first available Step Preset (for example Step 1 Preset), making it the next step (Next Sequencer Step, I:e.5/8–15). The pulse counter must count one pulse beyond the Step Preset (for example Step 1 Preset) before the first Valid Step (for example Step 1) is reached.

For example, if Step 2 Preset (M0:e.18) contains a value of 99, the step is reached one count after the Accumulated Count equals 99. If the pulse counter is incrementing, the step is reached when the Accumulated Count equals 100. If the pulse counter is decrementing, the step is reached when the Accumulated Count equals 98.

The order of the Valid Steps is from low to high, as defined in the Valid Steps field. If steps 1 and 3 are valid (enabled), step 1 will be reached before step 3 regardless of the pulse counter value. Step 3 will be reached only after the following conditions are satisfied:

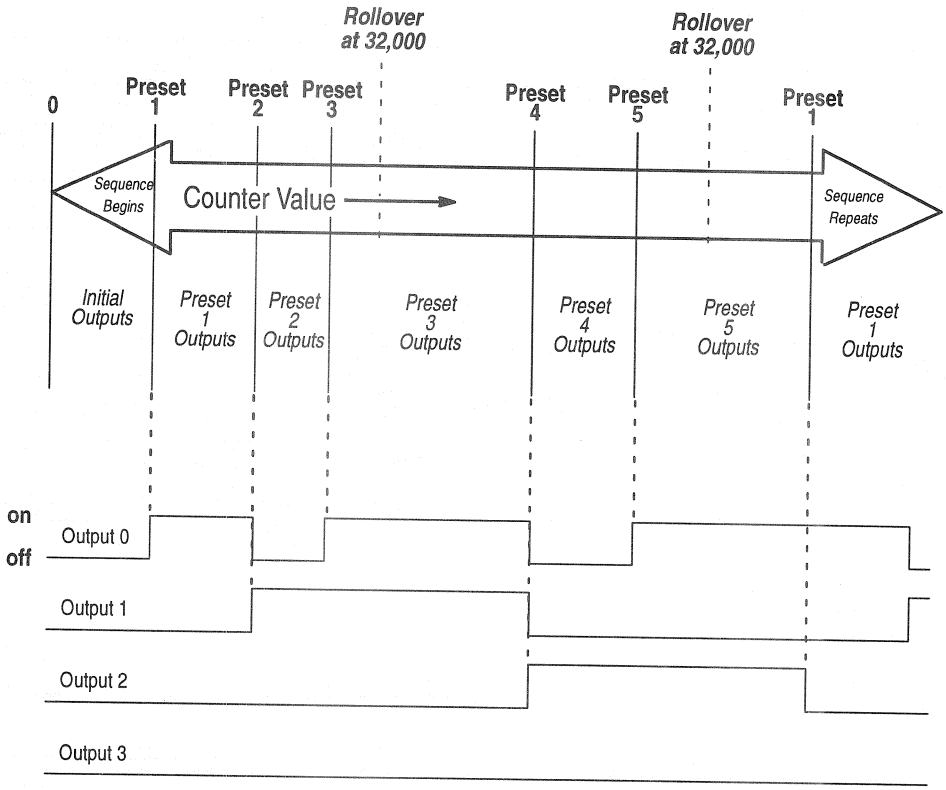
- Step 1 has been reached.
- The Accumulated Count is one step past the Step 3 Preset Value.

When step 3 is reached, the Step 3 Output pattern (M0:e.5/0–7) is applied to the Physical and Soft Outputs. The Step 3 Output pattern (M0:e.5/0–7) will be valid until the next Valid Step (step 1) is reached.

Unlike the Range and Rate Modes, the sequencer will not fall back to a previous step just because the pulse counter again reaches one count beyond the associated Step Preset. The sequencer is only looking for the Next Sequencer Step (I:e.5/8–15) in the sequence. The Next Sequencer Step Preset is located at I:e.7.

An example of sequencer operation with a ring counter is shown below. Here, the sequencer steps through 5 output patterns. This example demonstrates that the sequence can be defined over several counter rollovers. It also assumes that the Maximum Count Value is set to 32,000.

Sequencer Mode with Ring Counter



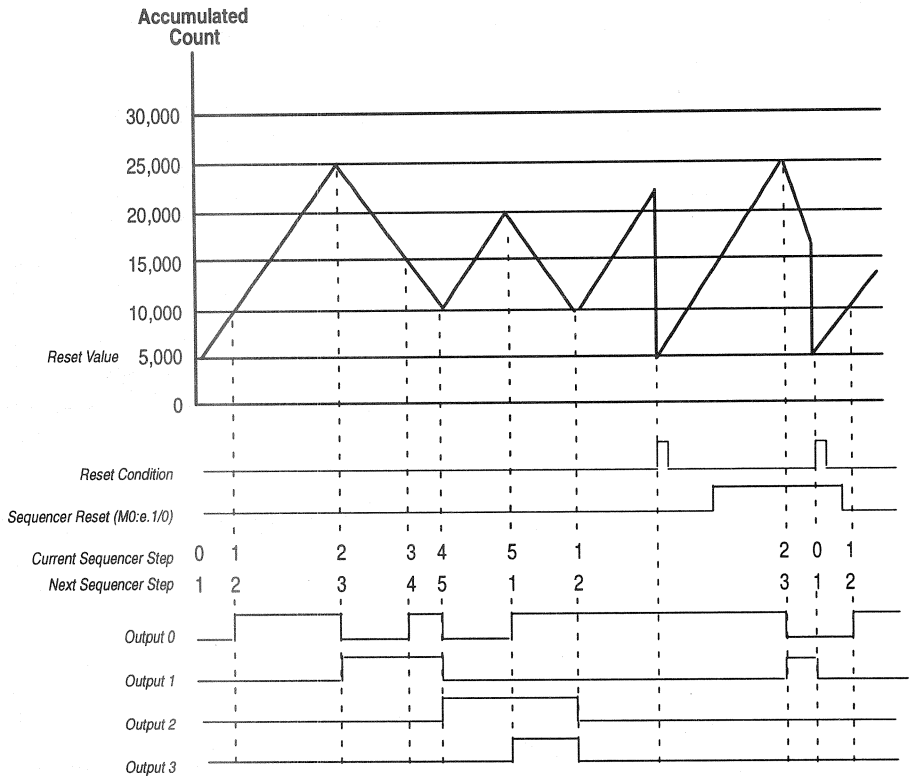
Preset Number	Desired Trigger	Preset Value	Outputs ① 7	6	5	4	3	2	1	0
Initial Output			0	0	0	0	0	0	0	0
1	10,000	9,999	0	0	0	0	0	0	0	1
2	20,000	19,999	0	0	0	0	0	0	1	0
3	27,000	26,999	0	0	0	0	0	0	1	1
4	15,000	14,999	0	0	0	0	0	1	0	0
5	25,000	24,999	0	0	0	0	0	1	0	1

Repeat Sequence

① Bits 0 – 3 are Physical Outputs. Bits 4 – 7 are Soft Outputs.

An example of Sequencer Mode with a linear counter is shown below.

Sequencer Mode with Linear Counter



Number	Desired Trigger	Preset Value	Outputs ① 7	6	5	4	3	2	1	0
Initial Outputs			0	0	0	0	0	0	0	0
1	10,000	9,999	0	0	0	0	0	0	0	1
2	25,000	24,999	0	0	0	0	0	0	1	0
3	15,000	15,001	0	0	0	0	0	0	1	1
4	10,000	10,001	0	0	0	0	0	1	0	0
5	20,000	19,999	0	0	0	0	1	1	0	1

① Bits 0 – 3 are Physical Outputs. Bits 4 – 7 are Soft Outputs.

Important: Resetting the counter does not reset the sequencer, unless the Sequencer Reset bit (M0:e.1/0) is set to1 prior to the occurrence of the reset.

Installation and Wiring

This chapter provides the following information:

- compliance to European Union directives
- dip switch and jumper location and settings
- module installation
- important wiring considerations
- input and outputs connections
- terminal block removal and wiring
- encoder wiring examples
- discrete devices and limit switch wiring examples

Compliance to European Union Directives

If this product has the CE mark it is approved for installation within the European Union and EEA regions. It has been designed and tested to meet the following directives.

EMC Directive

This product is tested to meet Council Directive 89/336/EEC Electromagnetic Compatibility (EMC) and the following standards, in whole or in part, documented in a technical construction file:

- EN 50081-2
  EMC – Generic Emission Standard, Part 2 – Industrial Environment
- EN 50082-2
  EMC – Generic Immunity Standard, Part 2 – Industrial Environment

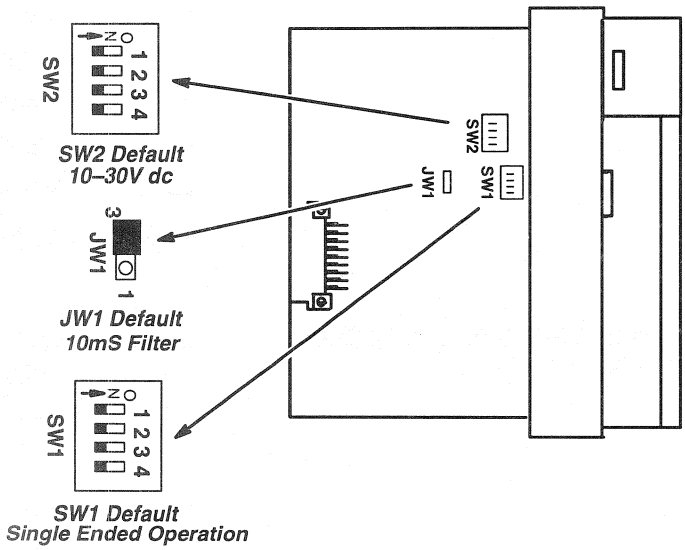
This product is intended for use in an industrial environment.

Dip Switch and Jumper Locations

Two dip switches (SW1 and SW2) and one jumper (JW1) are located on the side of the module.

- SW1 selects the type of input (single ended or differential).
- SW2 selects the output voltage range (4.5–10V dc or 10–30V dc).
- JW1 selects the filtering rate (300 µs or 10 ms) used to debounce the limit switch input.

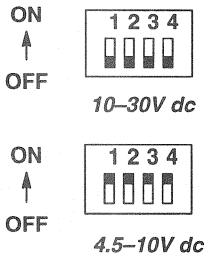
Default settings are shown below:



ATTENTION: Use a small screwdriver to change dip switch positions. Graphite from pencils will damage the switch.

SW2 Settings

Select an output voltage range that coincides with your supply voltage. The selections are 4.5–10V dc or 10–30V dc.



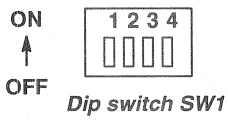
Switch	1	2	3	4
Output	0	1	2	3

ATTENTION: *All* switches of SW2 must be ON or *all* switches must be OFF. Permanent damage may result if some are ON and some are OFF.

Operating in the 10–30V dc range with the switches set for the 4.5–10V dc range will damage the module.

SW1 Settings

Select an input connection, single ended or differential.



Switch	1	2	3	4
Channel	A	B	Z	not used

Position	Input connection	Input ON range
ON	differential	2.8–4.5V dc
OFF	single-ended	3.1–5.5V dc

It is possible to configure different inputs in different modes. For example, input A (CHA) can be configured as differential and input Z (CHZ) can be configured as single ended.

JW1 Settings

Select 300 µs or 10 ms filtering to debounce the limit switch input. Position the jumper as follows:

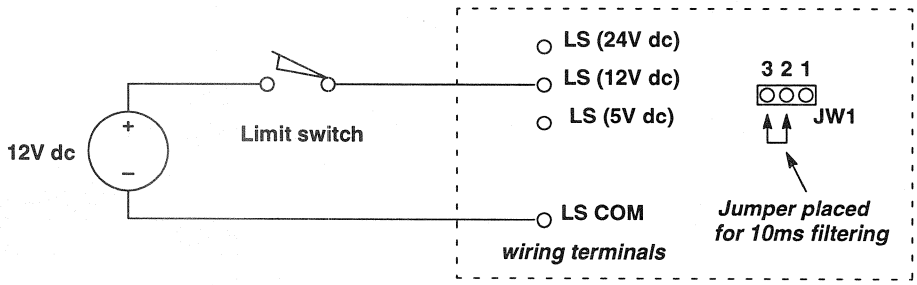
10 ms filter *300 µs filter*

The LS input allows you to make a direct connection to nominal voltage levels of 5, 12, or 24V dc. The ON voltage ranges are as follows:

Wiring terminal	ON range
LS (24V dc)	16.5–30V dc
LS (12V dc)	9.4–10.5V dc
LS (5V dc)	3.8–5.5V dc

Limit switch ON ranges

The figure below indicates how to connect a limit switch and 12V dc supply to the module. Jumper JW1 is placed for a 10 ms debounce.



This input is intended for connection to a limit switch used to reset the counter. The LS input can be used alone as a reset or in combination with the Z input, or Soft Reset (refer to M0:e.1/5–7).

ATTENTION: Only connect one LS input range at a time. Otherwise, the module will be damaged.

Installing the Module

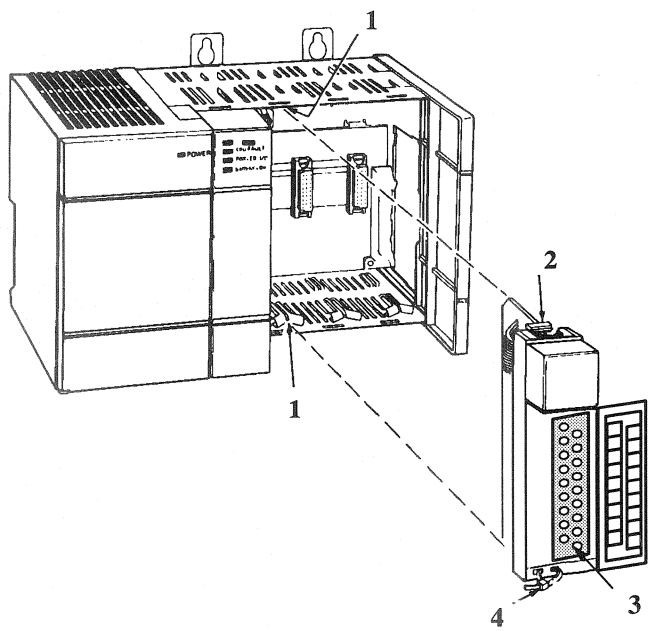
Installation procedures for this module are the same as any other discrete I/O or specialty module.

Important: Set the dip switches before installing the module.

ATTENTION: Disconnect power before attempting to install, remove, or wire the module.

Make sure your SLC power supply has adequate reserve current capacity. The module requires 320 mA at 5 volts.

1. Align the full sized circuit board with the rack card guide. The first slot (slot 0) of the first rack is reserved for the CPU.
2. Slide the module into the rack until the top and bottom latches are latched. To remove the module, press the releases at the top and bottom of the module and slide it out.
3. Make sure the removable terminal wiring block is attached to the module and all wires are connected to the terminal block.
4. Insert the cable tie in the slots and secure the cable.
5. Cover all unused slots with the Card Slot Filler, Catalog Number 1746-N2.



Important Wiring Considerations

Use the following guidelines when planning the system wiring for the module:

- Install the SLC 500 system in a NEMA rated enclosure.
- Disconnect power to the SLC processor and the module before wiring.
- Make sure the SLC 500 system is properly grounded.
- Group this module and low voltage DC modules away from AC I/O or high voltage DC modules.
- Shielded cable is required for high speed input signals A, B, and Z. We recommend Belden 9503 or equivalent for lengths up to 305 m (1000 ft).
- When the LS input is driven by an electromechanical device, route the wiring away from other inputs. In addition, JW1 should be set for the 10 ms filter.
- When the LS input is driven by a solid state device, use a shielded cable. You *do not* have to route the cable away from other inputs.
- Shields should be grounded only at the end of the signal source end of the cable. Ground the shield to the case of the signal source, so energy coupled to the shield will not be delivered to signal source's electronics.

Input and Output Connections

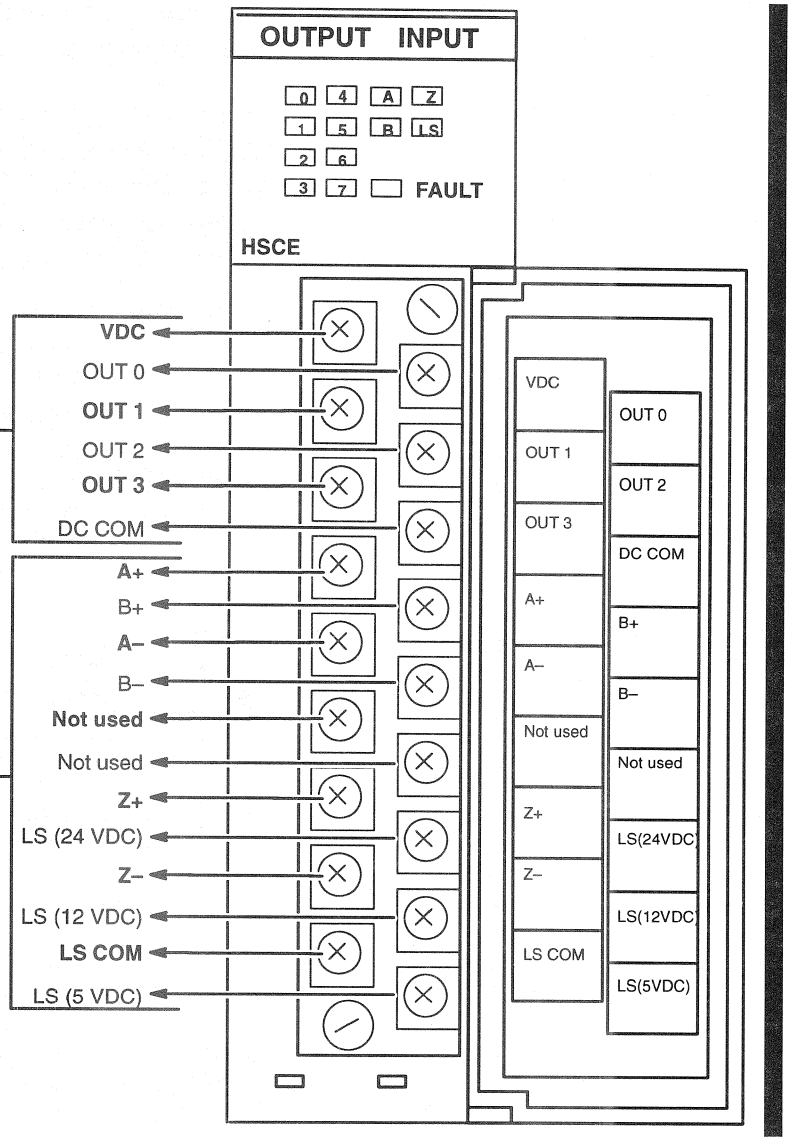
Input and output wiring terminals are located on the front of the module, behind the terminal cover. When you connect input and output devices, you will also be concerned with the settings of dip switch SW1 (input connections), dip switch SW2 (output connections), and jumper JW1 (limit switch input connections). The location and description of these are shown on page 3–3.

Discrete Output Wiring

NOTE: VDC must be externally supplied by the user. See page 3–8 for output wiring.

Limit Switch and Encoder Input Wiring

See pages 3–11 through 3–15 for input wiring.



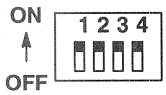
ATTENTION: Do not use incandescent lamps as output indicators. The high peak inrush current required to heat the filament can damage the module's output circuits. Use LED type indicators that satisfy the output circuit ratings, such as Allen-Bradley 800A and 800T LED indicators.

Outputs

The module provides four Physical Outputs. They can be controlled by the module when certain counter conditions are met, or they can be controlled from the user program (refer to M0:e.0 in chapter 4).

The outputs are bipolar transistors connected in a sinking (open collector sinking) configuration. When the output is energized, it sinks the current.

You can select an output voltage range of 4.5–10V dc or 10–30V dc. Refer to appendix A for the maximum current specs for each voltage range. Dip switch SW2, located on the PC board, is used to select the voltage range. The figure below identifies the switches and indicates how to set them.



Dip switch SW2

ON position. Move in direction of arrow.

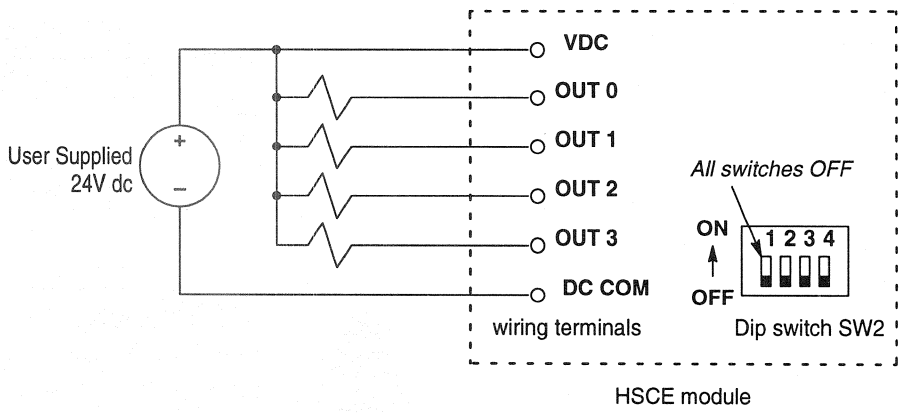
OFF position. Move in opposite direction of arrow.

Switch	1	2	3	4
Output	0	1	2	3

Position	Output voltage range
ON	4.5–10V dc
OFF	10–30V dc

ATTENTION: *All* switches of SW2 must be ON or *all* switches must be OFF. Permanent damage may result if some are ON and some are OFF.

The figure below indicates wiring connections for four 24V dc outputs. Switches of SW2 are OFF for this output voltage.



The outputs are *not* electrically isolated from each other. (They are referenced to the same output common terminal.) However, outputs are isolated from the rest of the circuitry to a level of 1500 volts.

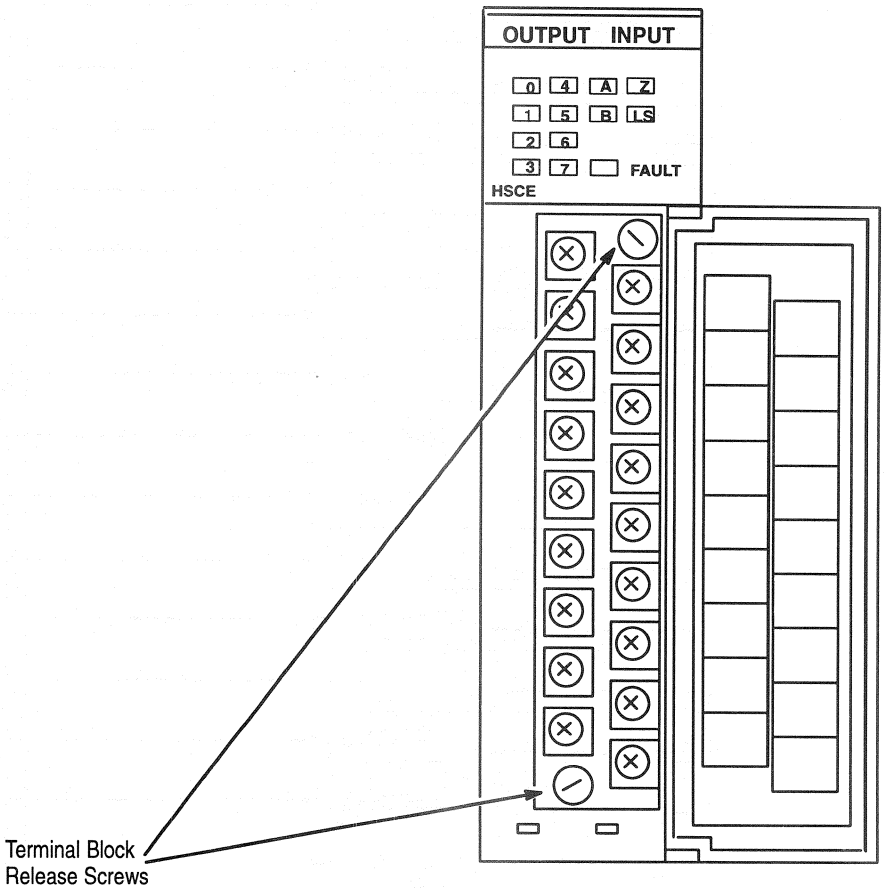
Removing the Terminal Block

The removable terminal wiring block eliminates the need to rewire a module if it is removed from the rack. Each terminal will accept two #14 AWG wires.

ATTENTION: Disconnect power before attempting to install, remove, or wire the removable terminal wiring block.

To avoid cracking the removable terminal block, alternate the removal of the slotted terminal block release screws.

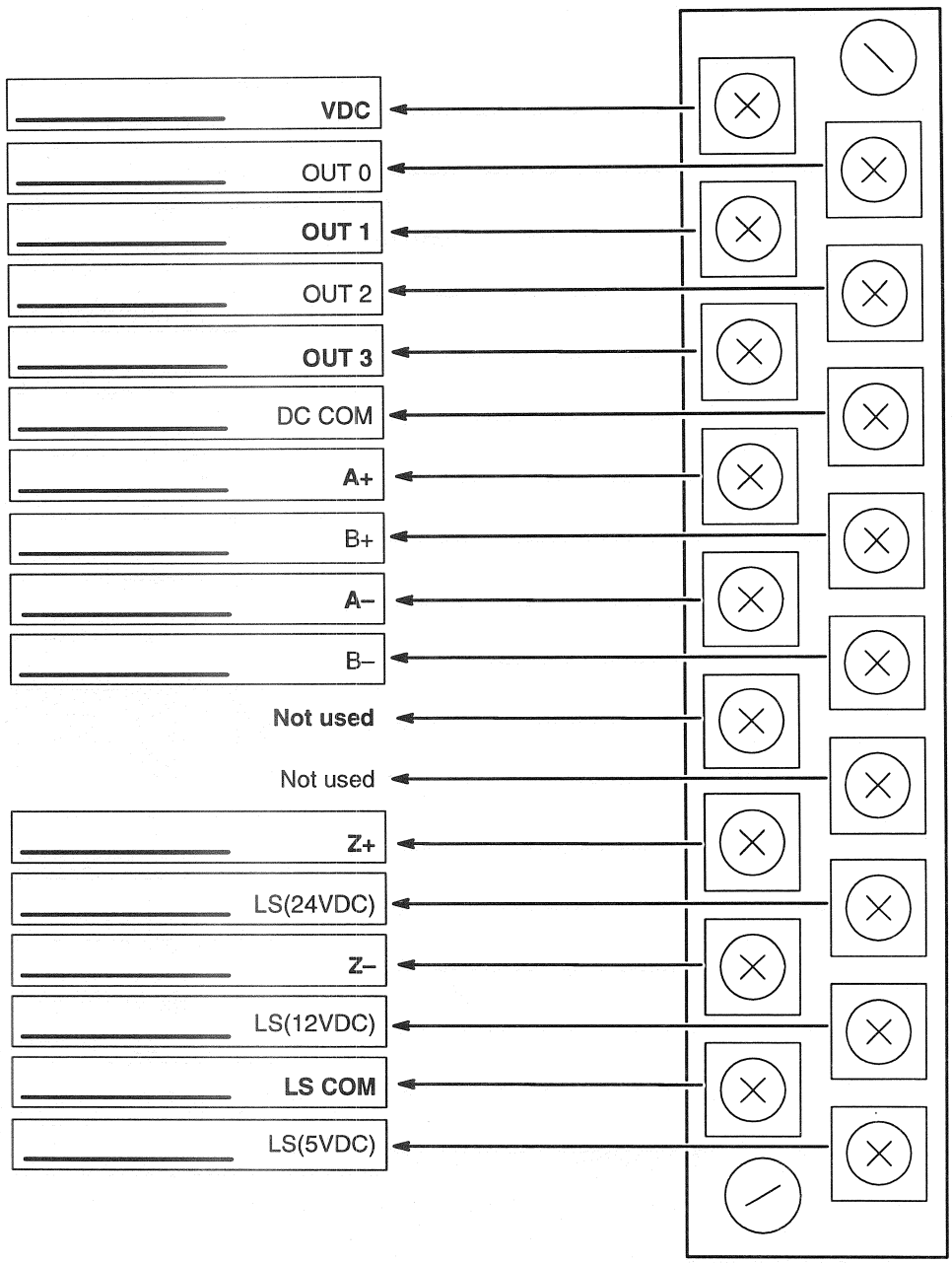
Remove the terminal block by turning the slotted terminal block release screws counterclockwise. The screws are attached to the terminal block, so it will follow as the screws are turned out.



Wiring the Removable Terminal Block

The terminal screws can be turned with flat or cross slot screwdrivers. Each screw should be turned tight enough to immobilize the wire's end. Over tightening can strip the terminal screw. The torque applied to each screw should not exceed 5.3 inch pounds.

Shown below, is a wiring template for the terminal block.

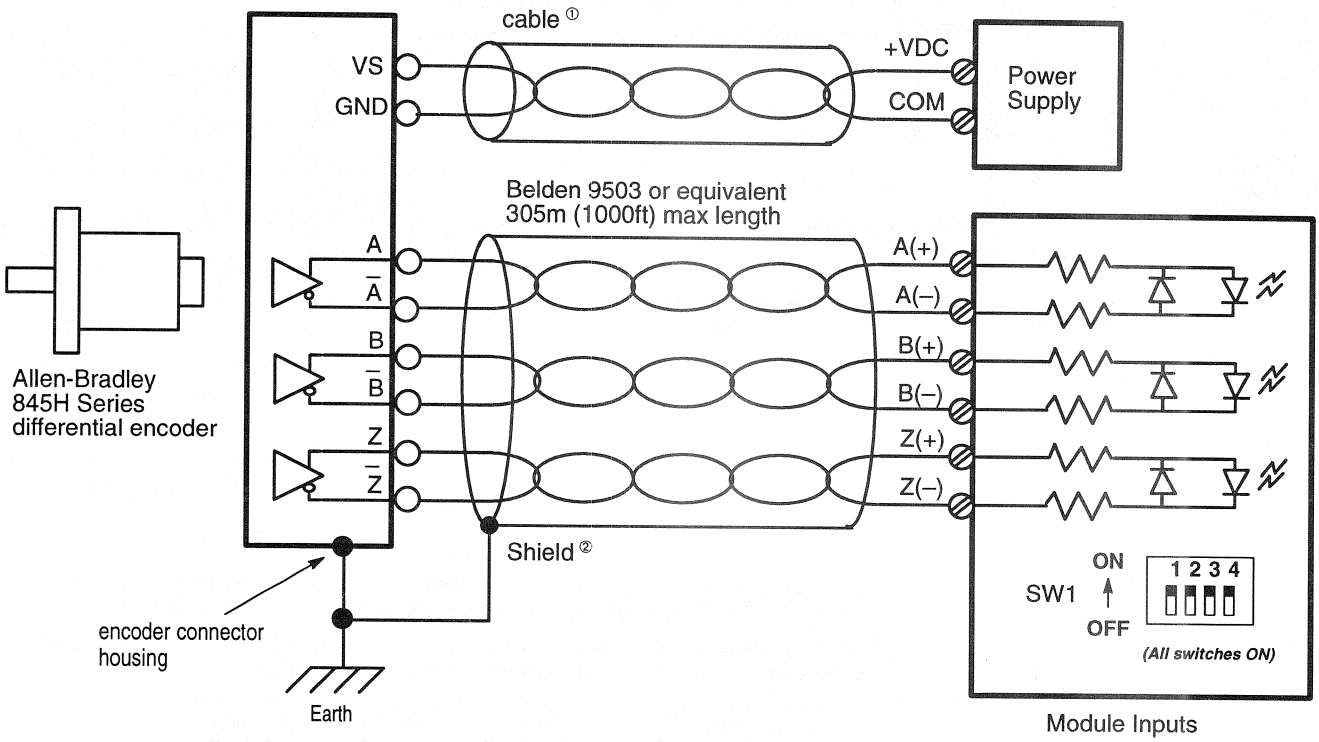


Encoder Selection

Differential encoders provide the best immunity to electrical noise. We recommend, whenever possible, to use differential encoders.

The wiring diagrams on the following pages are provided to support the Allen-Bradley encoders you may already have.

Differential Encoder Wiring

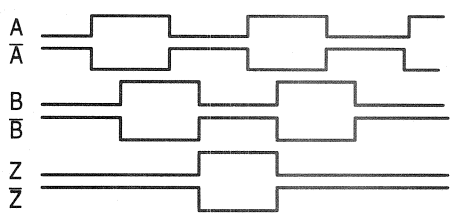


① Refer to your encoder manual for proper cable type and length.

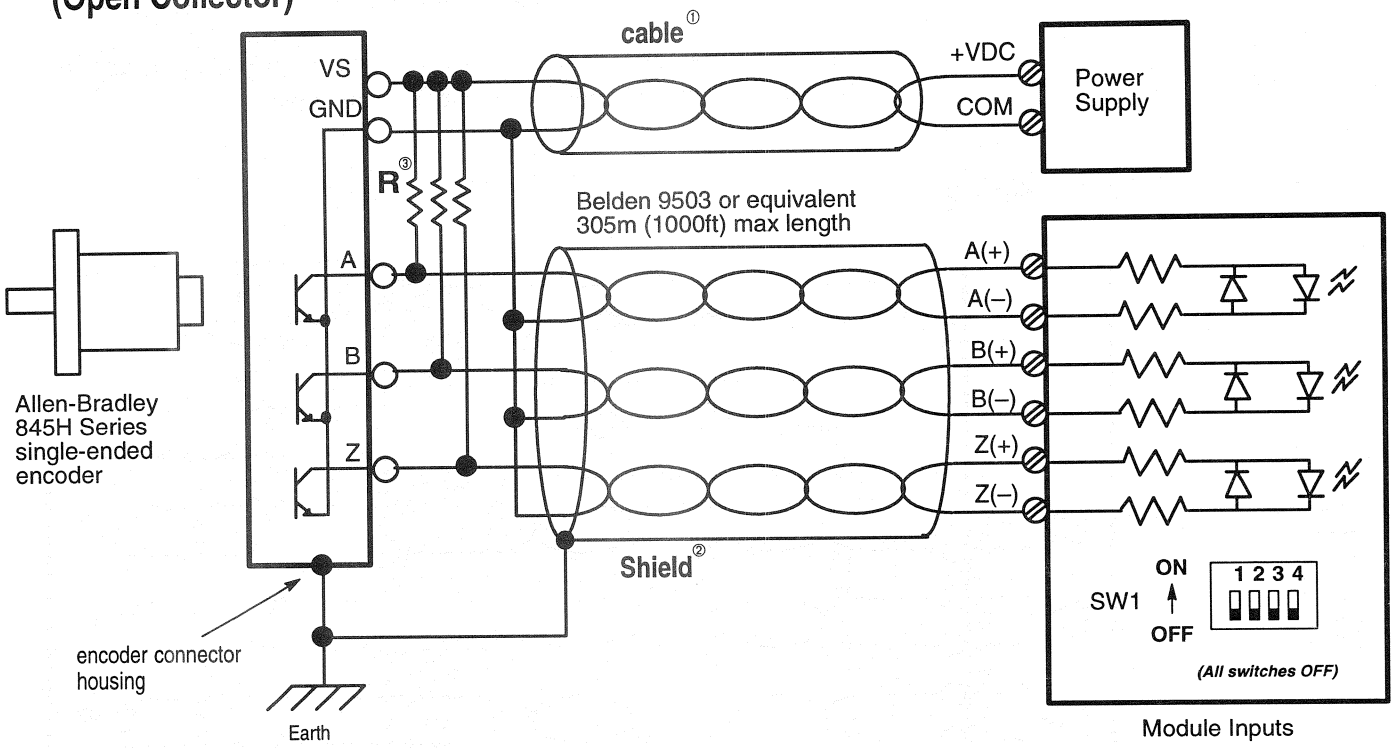
② Due to the topology of the module's input circuits, terminating the shield at the encoder end provides the highest immunity to EMI interference. Connect EARTH ground directly to the encoder connector housing.

Differential Encoder Output Waveforms

The illustration below shows the different encoder output waveforms. If your encoder matches these waveforms, the encoder signals can be directly connected to the associated screw terminals on the module. For example, the A lead from the encoder is connected to the module's A+ screw. If your encoder does not match these waveforms, some wiring modifications may be necessary. Refer to appendix C for a description of these modifications.



Single-Ended Encoder Wiring (Open Collector)



① Refer to your encoder manual for proper cable type and length.

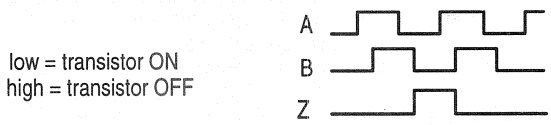
② Due to the topology of the module's input circuits, terminating the shield at the encoder end provides the highest immunity to EMI interference. Connect EARTH ground directly to the encoder connector housing.

③ The pullup resistor (R) value depends on the power supply value (VS). The table below lists the resistor values for typical power supply values. These resistors must be located at the encoder end of the cable.

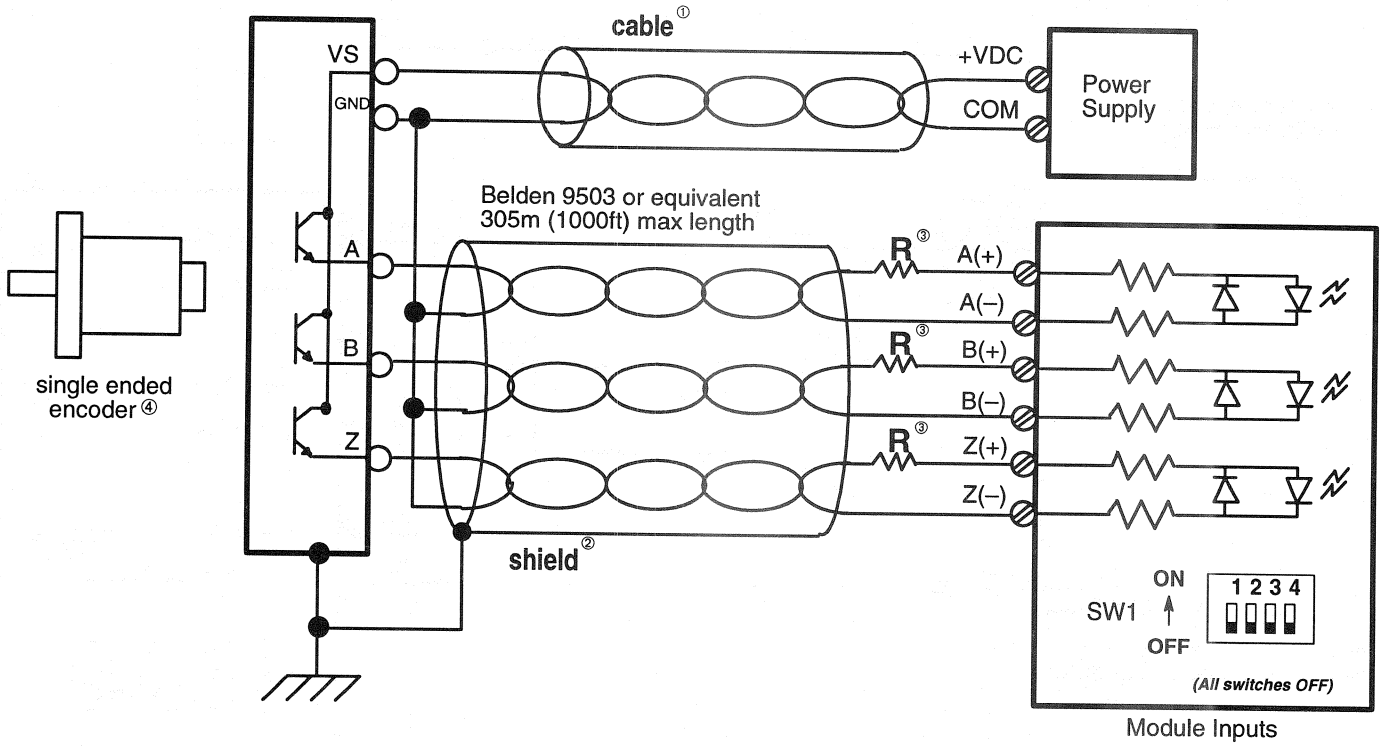
VS Value	R Value	Maximum Output Leakage
+5V dc	150 ohm 1/4W 5%	6.3 mA
+12V dc	1800 ohm 1/4W 5%	1.5 mA
+24V dc	4700 ohm 1/4W 5%	1.2 mA

Single-Ended Encoder Output Waveforms

The figure below shows the single-ended encoder output waveforms. When the waveform is low, the encoder output transistor is ON.



Single-Ended Encoder Wiring (Sourcing)



① Refer to your encoder manual for proper cable type and length.

② Due to the topology of the module's input circuits, terminating the shield at the encoder end provides the highest immunity to EMI interference. Connect EARTH ground directly to the encoder connector housing.

③ The resistor (R) value depends on the power supply value (VS). The table below lists the resistor values for typical power supply values. These resistors must be located at the module end of the cable.

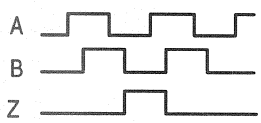
VS Value	R Value	Maximum Output Leakage
+5V dc	no resistor needed	100 µA
+12V dc	1800 ohm 1/4W 5%	100 µA
+24V dc	4700 ohm 1/4W 5%	100 µA

④ The Allen-Bradley 845H sourcing encoder is not compatible with this module.

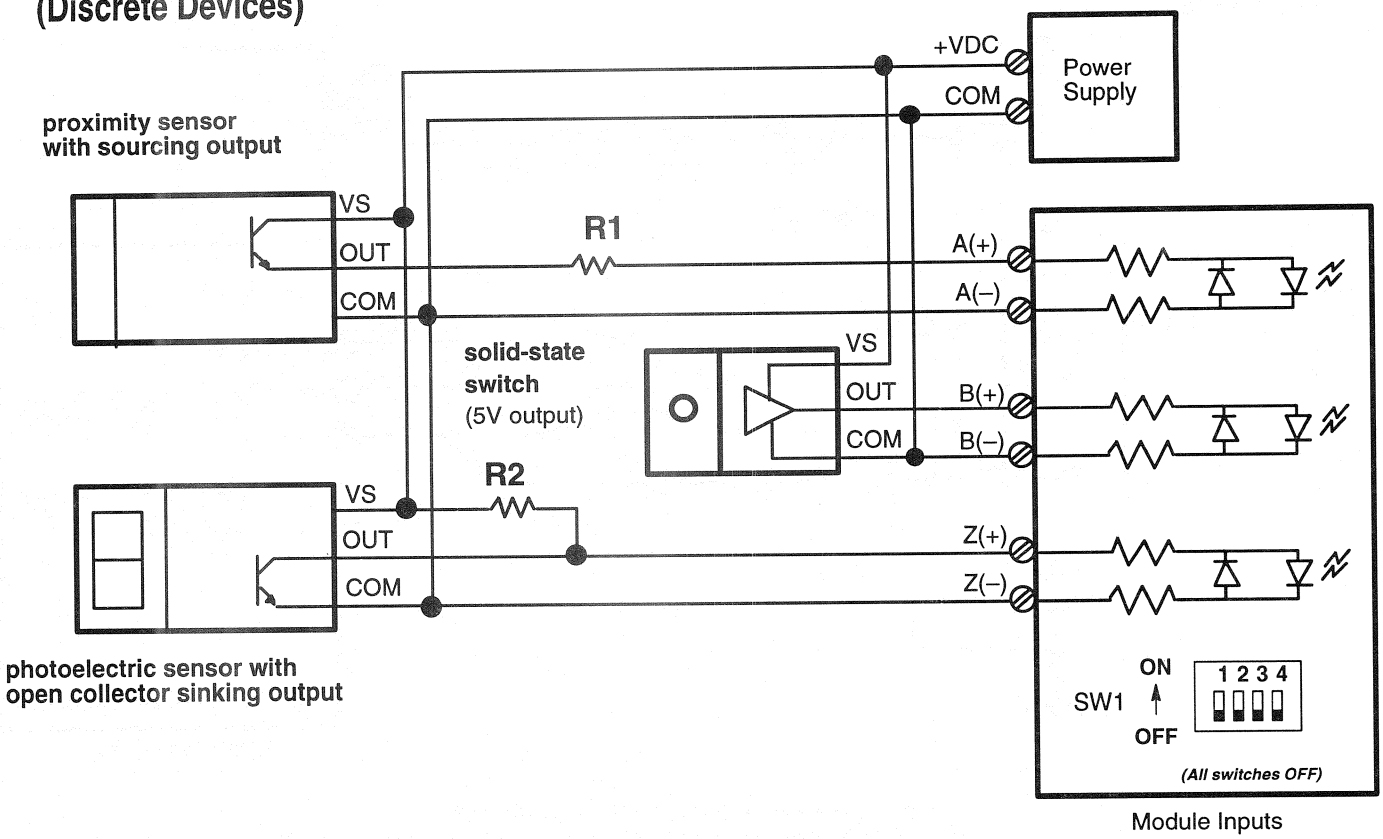
Single-Ended Encoder Output Waveforms

The figure below shows the single-ended encoder output waveforms. When the waveform is low, the encoder output transistor is OFF.

low = transistor OFF
high = transistor ON



Single-Ended Wiring (Discrete Devices)



Notes

1. This diagram shows the sensors operating from a common power supply. Separate power supplies for each circuit can be used.

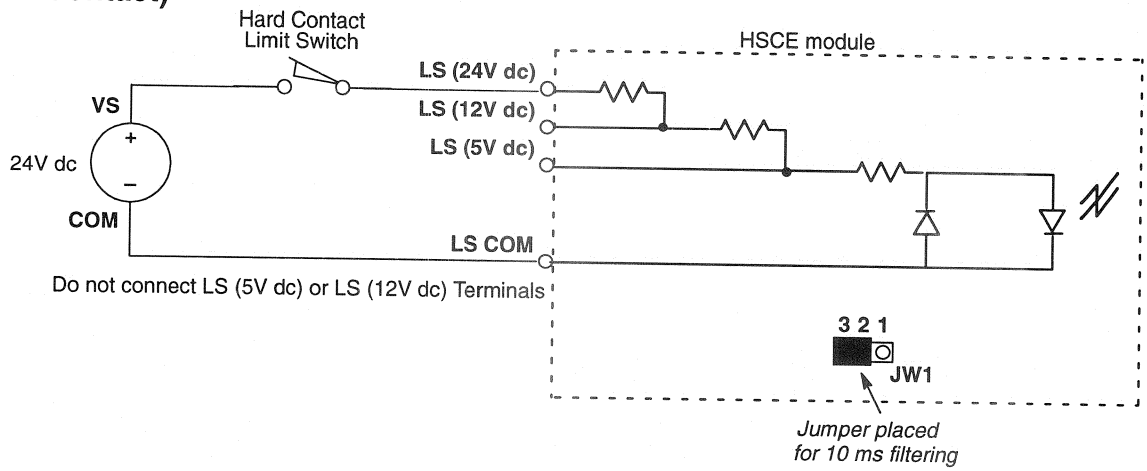
2. The resistor (R1) value depends on the power supply value (VS). The table below lists the resistor values for typical power supply values. These resistors must be located at the module end of the cable.

VS Value	R1 Value	Maximum Output Leakage
+5V dc	no resistor needed	100 µA
+12V dc	1800 ohm 1/4W 5%	100 µA
+24V dc	4700 ohm 1/4W 5%	100 µA

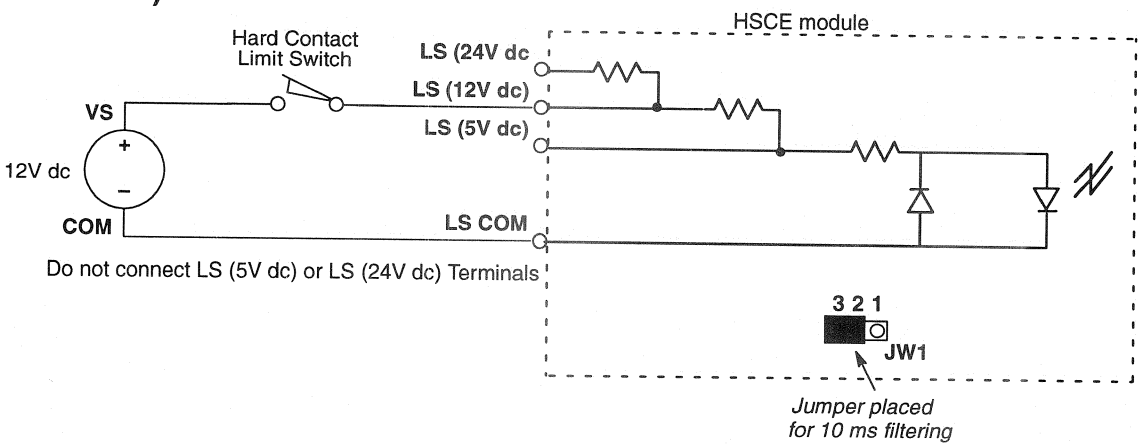
3. The pullup resistor (R2) value depends on the power supply value (VS). The table below lists the resistor values for typical power supply values. These resistors must be located at the sensor end of the cable.

VS Value	R2 Value	Maximum Output Leakage
+5V dc	150 ohm 1/4W 5%	6.3 mA
+12V dc	1800 ohm 1/4W 5%	1.5 mA
+24V dc	4700 ohm 1/4W 5%	1.2 mA

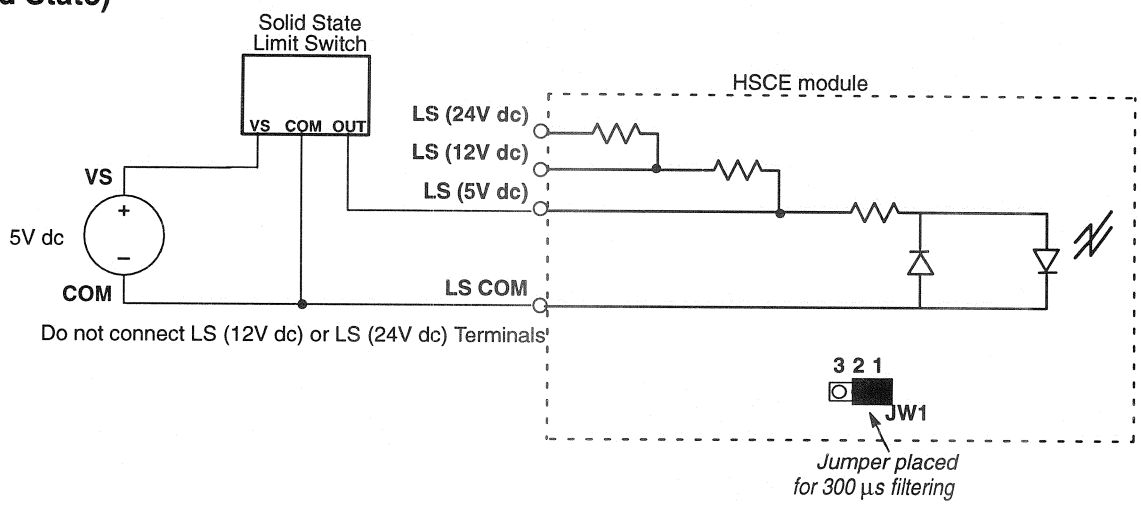
Limit Switch Wiring (24V dc Hard Contact)



Limit Switch Wiring (12V dc Hard Contact)



Limit Switch Wiring (5V dc Solid State)



Configuration and Programming

This chapter contains the Output, Input and M0 file information.

- a discussion of Dynamic and Static Parameters
- SLC processor configuration steps for use with APS
- SLC processor configuration steps for use with an HHT
- M0 file contents for range and rate modes
- output data file contents for range and rate mode operation
- input data file contents for range and rate mode operation
- M0 file contents for sequencer mode operation
- output data file contents for sequencer mode operation
- input data file contents for sequencer mode operation

Configuration Worksheets

To assist you in the configuration of your SLC processor and the monitoring of your module, configuration worksheets are contained in appendixes E and F. Appendix E contains worksheets for Range and Rate Mode operation. Appendix F contains worksheets for Sequencer operation. Do not remove the worksheets from the manual, photocopy them so they can be re-used.

The worksheets are used in chapter 6, Application Examples. In addition, the Configuration Data Tables are shown for comparison to the worksheets.

Dynamic and Static Parameters

This chapter identifies parameters as Dynamic and Static. Dynamic Parameters immediately update the operating conditions. They do not disrupt counter operation. Only one Dynamic Parameter should be changed at a time.

Static Parameters can only be changed when the Function Control bit is reset to 0. They will not alter operating conditions until the Function Control Bit is set to 1. A module fault occurs when you try to change a static parameter while the Function Control bit is set to 1.

SLC Processor Configuration Using APS

Your SLC processor can be programmed with APS (Advanced Programming Software) or an HHT (Hand-Held Terminal). Although the configuration steps are similar, they are not identical.

The following steps are provided for the modification of an existing user program with APS. For information on M Files, refer to appendix B.

Important: The High-Speed Counter module does not support the interrupt capability described in appendix B.

ATTENTION: If you are using APS version 2.0 or 3.0 with the High-Speed Counter module, refer to appendix D for important procedures you must follow. Failure to adhere to these instructions could result in unexpected input and/or output operation.

1. Locate an open slot in your chassis. The module can only be used with SLC 5/02 (or later) processors.
2. Assign your SLC processor (if you haven't already):

   A. Press OFFLINE PRG/DOC (F3), PROCSSR FUNCTNS (F1), and then CHANGE PROCSSR (F1).

   B. Press SELECT PROC (F2) to select a processor.
3. Assign the module to an open slot:

   A. Press CONFIGR I/O (F5).

   B. Highlight an open slot and press MODIFY SLOT (F5).

   C. If you are using **APS v2.x** or earlier:

      (1) Highlight the last entry entitled OTHER and press [ENTER].

      (2) Enter module ID Code 12705.

      (3) Create 8 input words when prompted by APS.

      (4) Create 1 output word when prompted by APS.

   D. If you are using **APS v3.x** or later:

      (1) Highlight 1746-HSCE and press [ENTER].

      (2) Create 8 input words when prompted by APS.

(3) Create 1 output word when prompted by APS.

4. Create 42 M0 file words.

   Important: You do not need to create any M1 file words or G file words to use the High-Speed Counter module.

   A. Press SPIO CONFIG (F9), ADVNCD SETUP (F5), and then M0 FILE SIZE (F5).

   B. Type 42 and press [ENTER].

   C. If the user program will not be directly controlling the outputs (O:e.0/0–7), set the number of scanned outputs to 0.

5. Module operation is determined by the information loaded to the M0 file (by the user program) from a data file. To load the module configuration to the M0 file, use a COP instruction with a bit file (#B) or integer file (#N) source, a destination of #M0:e.0, and a length of 42.

6. Use the Data Monitor function to enter parameters into the Bit (#B) or Integer (#N) file. Use F1 to change between binary and decimal.

SLC Processor Configuration Using HHT

Your SLC processor can be programmed with APS (Advanced Programming Software) or an HHT (Hand-Held Terminal). Although the configuration steps are similar, they are not identical.

The following steps are provided for the modification of an existing user program, with an HHT. For information on M files, refer to appendix B.

Important: The High-Speed Counter module does not support the interrupt capability described in appendix B.

1. Locate an open slot in your chassis. The module can only be used with SLC 5/02 (or later) processors.

2. Assign your SLC processor (if you haven't already).

   A. Press PROGMAINT (F3), [ENTER], SEL_PRO (F2), and TYPE (F1).

   B. Select the processor type with the cursor and press [ENTER] and [ESC].

3. Assign the module to an open slot.

   A. Press EDT_I/O (F3) and then select an open slot with the cursor.

B. Press MOD_SLT (F2) and OTHER (F3).

C. Enter Module ID Code 12705.

D. Create 1 output word.

E. Create 8 input words.

4. Create 42 M0 file words.

Important: You do not need to create any M1 file words or G file words to use the High-Speed Counter module.

A. Press ADV_SET (F5) and ADV_SIZ (F4).

B. Press [ENTER] four times.

C. Type 42 and press [ENTER].

D. If the user program will not be directly controlling the outputs (O:e.0/0–7), set the number of scanned outputs to 0.

5. Module operation is determined by the information loaded to the M0 file (by the user program) from a data file. To load the module configuration to the M0 file, use a COP instruction with a bit file (#B) or integer file (#N) source, a destination of #M0:e.0, and a length of 42.

6. Use the EDT_DAT function to enter parameters into your Bit or Integer file.

Important: The HHT has a default radix of binary for the Bit file (#B) and integer for the Integer file (#N). Radixes cannot be changed.

Important: Reserved bits must be reset to 0.

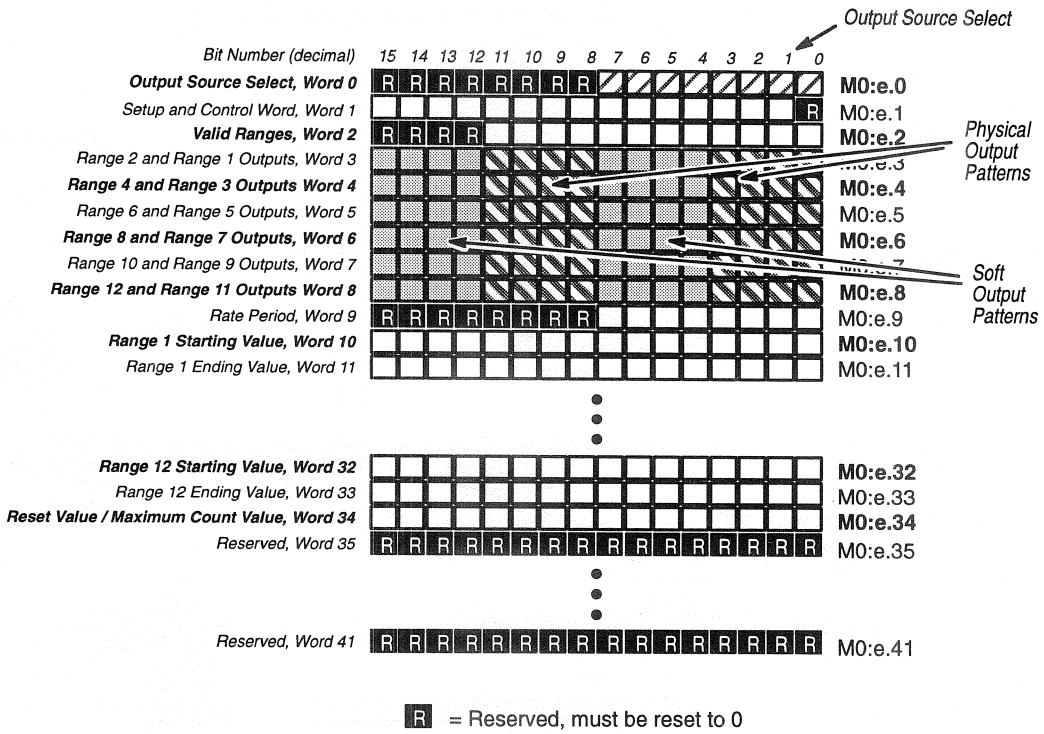
M0 File Words – Range and Rate Modes

For more information on M0 files, refer to appendix B.

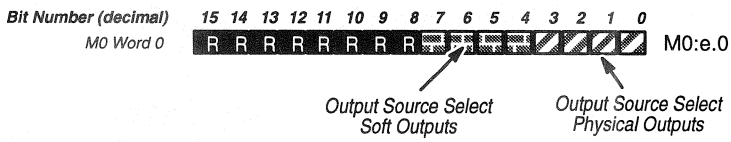
Important: The High-Speed Counter module does not support the interrupt capability described in appendix B.

Appendix E contains worksheets for Range and Rate Mode operation.

Important: Reserved bits must be reset to 0.



M0:e.0 Output Source Select



M0:e.0 Bits 0 through 7 – Output Source Select (Dynamic)

Bits 0, 1, 2, and 3 represent the Physical Outputs. Bits 4, 5, 6, and 7 represent the Soft Outputs.

The status of these bits determines whether an output is controlled by the module (when the Function Control bit is set to 1), or by the user program.

Output Source Select (bits 4–7)	Output Status
0	Output is under module control
1	Output is under user program control

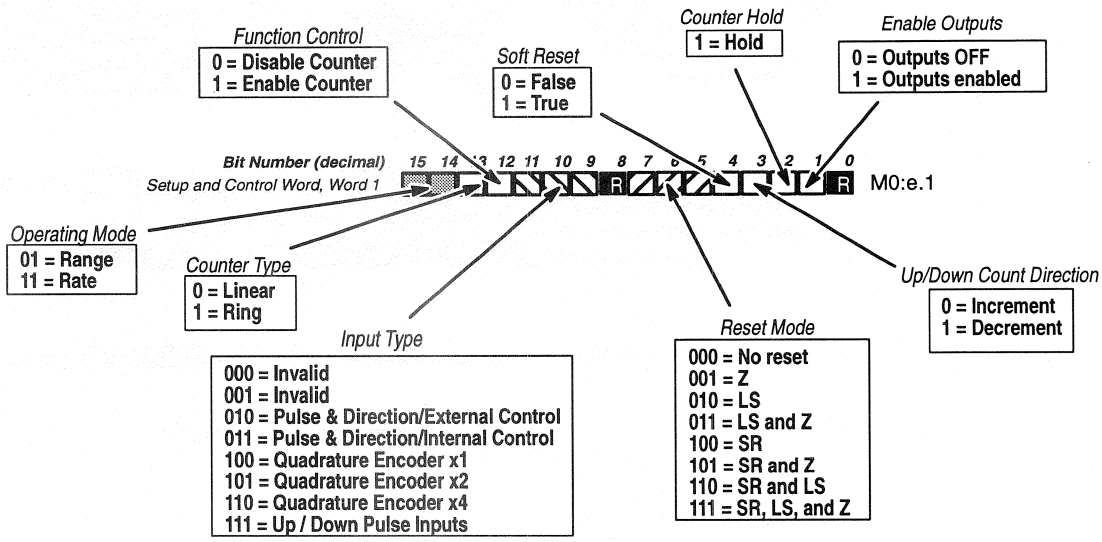
A logic 0 in any of these positions means that the corresponding output is under module control. A logic 1 means that the corresponding output is under user program control (refer to *O:e.0/0–7 Direct Outputs*).

The Output Source Select bit values are dynamic and can be changed by the user program at any time.

MO:e.0 Bits 8 through 15

Bits 8 through 15 are reserved and must be reset to 0.

M0:e.1 Setup and Control Word



R = Reserved, must be reset to 0

M0:e.1 Bit 0

Bit 0 is reserved and must be reset to 0.

M0:e.1 Bit 1 – Enable Outputs (Dynamic)

This bit enables the Physical and Soft Outputs (O:e.0/0–7). When the bit is logic 0, outputs are turned off regardless of the state of the module or the Direct Output fields. You must set this bit (to 1) to allow the module to independently control the outputs, or to allow direct output control by the user program.

Enable Outputs (bit 1)	Output Status
0	Outputs are OFF
1	Outputs are enabled

The Output Source Select field (M0:e.0/0–7) determines whether the module or user program controls the outputs.

M0:e.1 Bit 2 – Counter Hold (Dynamic)

When set to 1, this bit prevents the pulse counter from counting input pulses. In addition, the Pulse Counter State bits in the Status Word (I:e.0/14–15) are set to Hold.

Counter Hold (bit 2)	Pulse Counter State
0	Pulses are passed to the pulse counter
1	Pulses are ignored

The Counter Reset function and Rate Measurement are not affected when the Counter Hold bit is set.

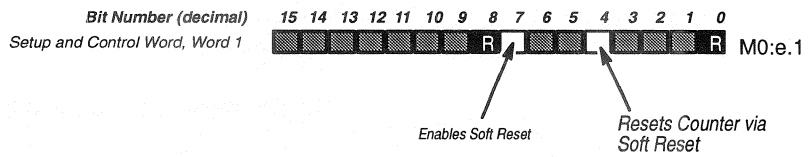
M0:e.1 Bit 3 – Up/Down Count Direction (Dynamic)

This bit allows you to control the direction of the count when the Pulse and Direction with Internal Control Input Type (M0:e.1/9–11) is selected. This bit has no meaning when any other input type is selected.

Up/Down Count Direction (bit 3)	Affect on Accumulated Count
1	Accumulated Count decrements with each count received on Input A
0	Accumulated Count increments with each count received on Input A

M0:e.1 Bit 4 – Soft Reset (Dynamic)

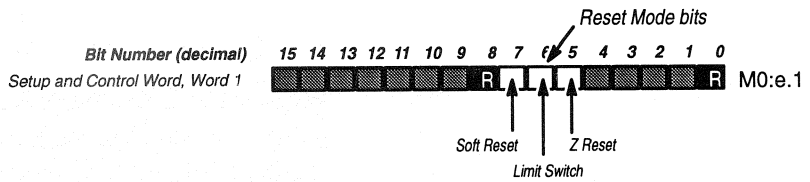
The Soft Reset bit can be used to reset the counter in combination with the physical reset signals. Setting this bit (to 1) resets the counter, via the Reset Mode bits, if Soft Reset (bit 7) is selected. The 0 to 1 transition of the Soft Reset condition (M0:e.1/5–7) resets the counter when configured to do so (refer to *Counter Reset Control* found in chapter 2).



Important: The Soft Reset bit must be held at 1 until the counter resets. The Reset Input bit (I:e.0/12) can be used to detect a counter reset.

M0:e.1 Bits 5,6,7 – Reset Mode (Static)

These bits allow you to select the device(s) that reset the counter. Bit 5 enables the Z reset, Bit 6 enables the limit switch reset, and bit 7 enables the soft reset, as shown below:



Setup and Control Word bits			Reset Condition is True
7	6	5	
0	0	0	Never
0	0	1	When Z is ON
0	1	0	When the limit switch is ON
0	1	1	When the limit switch and Z are ON
1	0	0	When the Soft Reset is 1
1	0	1	When the Soft Reset is 1 and Z is ON
1	1	0	When the Soft Reset is 1 and limit switch is ON
1	1	1	When the Soft Reset is 1, limit switch and Z are ON

The reset of the counter is edge triggered. It occurs only when all of the conditions specified become true. If multiple conditions are selected, the counter is reset on the last event's 0 to 1 transition. For example, if Z and LS are selected (011), Z by itself will not trigger the reset. Z and LS must both be ON.

Important: The time it takes for the counter to reset depends upon the value it resets to. If the reset value is zero, the counter resets immediately on the false to true edge of the reset condition without losing subsequent counts. If the reset value is nonzero, there is a delay of up to 500 µs before the reset value is loaded. Count pulses can be lost if they happen during the delay time. Refer to *Timing Information* in appendix A.

M0:e.1 Bit 8

Bit 8 is reserved and must be reset to 0.

M0:e.1 Bits 9,10,11 – Input Type (Static)

You configure this field to define the counter input type you are using:

Setup and Control Word bits			Input Type
11	10	9	
0	0	0	Invalid – configuration error
0	0	1	Invalid – configuration error
0	1	0	Pulse and Direction w/External Control
0	1	1	Pulse and Direction w/Internal Control
1	0	0	Quadrature Encoder Input – X1
1	0	1	Quadrature Encoder Input – X2
1	1	0	Quadrature Encoder Input – X4
1	1	1	Up/Down Pulse Inputs

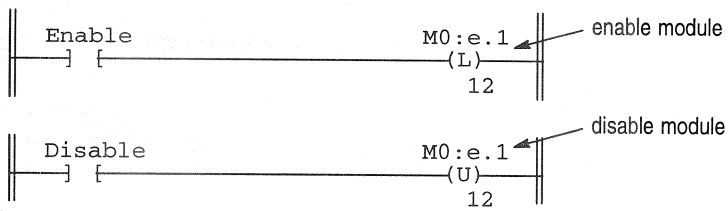
The input type you select determines how the A and B inputs cause the module's counter to increment and decrement. For all three input types, the Z input can be used to force a counter reset. The A, B, and Z inputs operate with input signals up to a maximum rate of 50 KHz.

M0:e.1 Bit 12 – Function Control (Dynamic)

This bit enables and disables the counter function.

Function Control bit	Function
0	Disable counter (except user program controlled outputs)
1	Enable counter

Important: The Function Control Bit must always be controlled by rungs in the ladder logic. Do not set the Function Control bit to 1 until all of your configured parameters are transferred. Never save the program with the Function Control bit set.



Static parameters can be changed when the Function Control Bit equals 0. Module operation will be altered upon the 0 to 1 transition of the Function Control bit.

When the Function Control bit changes from 1 to 0:

1. All outputs under module control are turned off (excluding outputs under user program control).
2. The pulse and rate counters are cleared and held at zero.

3. The following data file fields are cleared:
   - Accumulated Count
   - Rate Period Count, Rate Measurement
   - Output Status
   - Ranges Active
4. The Pulse Counter State field identifies the stopped condition.
5. Configuration errors are cleared.

The user program can change the Function Control bit dynamically in either the run or test modes to reconfigure or control the operation. You can change the preset or range information at any time independent of this bit. Refer to *Timing Information* located in appendix A.

M0:e.1 Bit 13 – Counter Type (Static)

This bit allows you to define the module's Counter Type:

Counter Type (bit 13)	Counter Type
0	Linear
1	Ring

M0:e.1 bits 14 and 15 – Operating Mode (Static)

These bits define the module's Operating Mode.

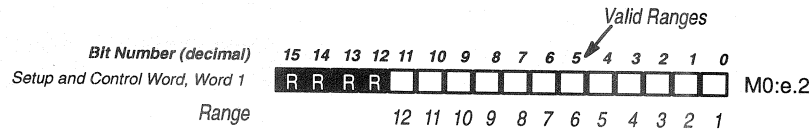
Operating Mode Bits		Operating Mode
15	14	
0	0	invalid
0	1	Range
1	0	Sequencer
1	1	Rate

Important: When operating in the Rate Mode, we recommend using the Ring Counter (M0:1/13) with a Maximum Count Value (M0:e.34) of 32,767. Doing so will allow the counter to roll over if the counts exceed 32,767.

When using the linear counter, an overflow error (I:e.0/13) will occur when the counts exceed 32,767.

M0:e.2 Valid Ranges (Dynamic)

The Range and Rate Modes support 12 different ranges. This word is used to enable Range Outputs fields.



M0:e.2 Bits 0 through 11 – Valid Ranges

Bits 0 through 11 represent ranges 1 through 12 respectively. When a bit is set to 1, the range it represents is enabled. When reset to 0, the range is disabled.

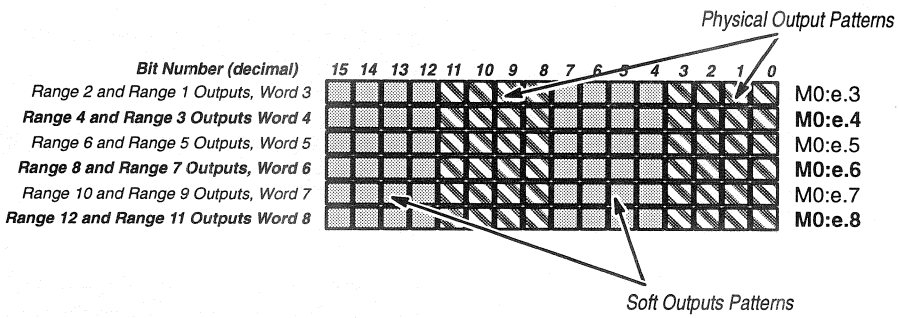
Valid Ranges (bits 0–11)	Corresponding Range
0	Range is disabled
1	Range is enabled

M0:e.2 Bits 12 through 15

Bits 12 through 15 are reserved and must be reset to 0.

M0:e.3 through M0:e.8 – Range 1 through 12 Outputs (Dynamic)

Use these words to program specific on/off output patterns. The Range 1 through Range 12 Outputs, shown below, are associated with Ranges 1 through 12 respectively. Each output field consists of 8 bits. The four lowest numbered bits correspond to the module's Physical Outputs. The four highest numbered bits correspond to the Soft Outputs.

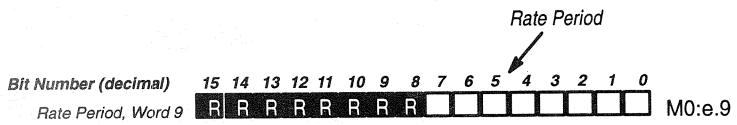


The Physical and Soft Output patterns are applied to the module outputs (terminals) and Outputs Status Word (I:e.4/8–15). When a Range Outputs bit is set to 1, the physical output will be energized if:

- the Accumulated Count (I:e.1) or Rate Measurement (I:e.3) is within the associated range
- Enable Outputs (M0:e.1/1) is true (if false, but the other conditions are true, the output bit will be set but the output will not be energized)
- the output is under module control (refer to Output Source Select M0:e.0/1–7)

For example, while in range 2, the Range 2 Outputs (M0:e.3) bits 8–11 are applied to the module's Physical Outputs 0–3. Bits 12–15 are applied to the Soft Output bits 4–7. Soft Output bits (I:e.4 /12–15) may be used in in your user program as event flags.

M0:e.9 Rate Period (Dynamic)



M0:e.9 Bits 0 through 7

This value represents the interval (Rate Period) of which the Rate Calculation will be performed.. The integer value entered in bits 0–7 can range from 1–255. It is multiplied by 10ms to obtain the actual Rate Period time. If reset to 0, a fault will occur. Refer to *Selecting the Rate Period Parameter* found in chapter 2.

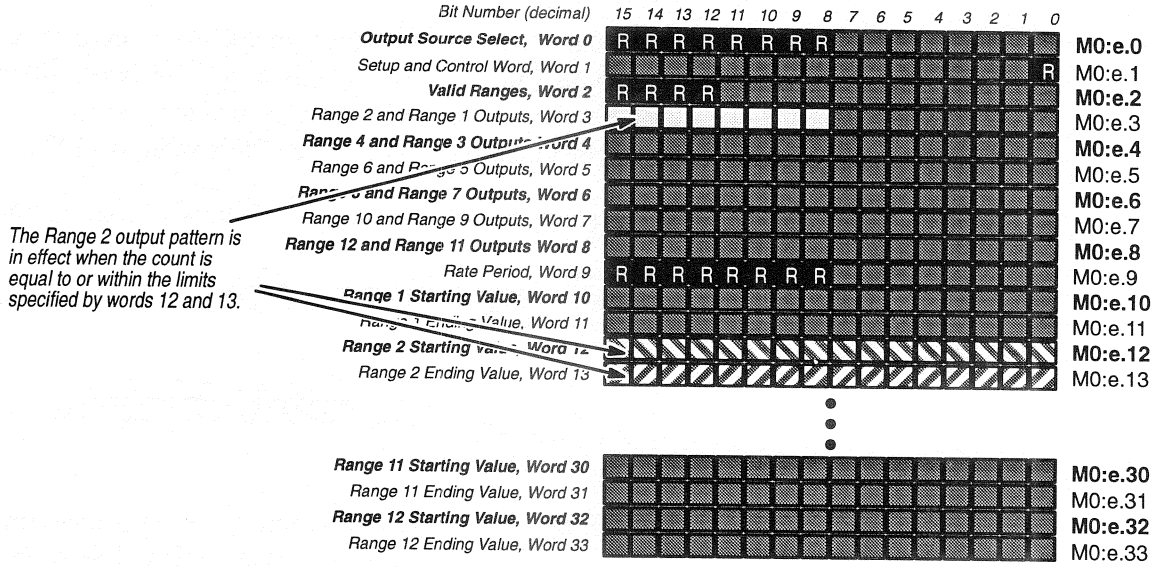
M0:e.9 Bits 8 through 15

Bits 8 through 15 are reserved and must be reset to 0.

M0:e.10 through M0:e.33 Starting/Ending Range Values (Dynamic)

The Range and Rate Mode each support 12 ranges and have a Range Starting Value and a Range Ending Value. Integer values are entered into the Range Starting and Ending Values.

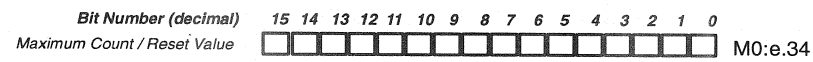
For example, when in Range Mode, Range 2 (M0:e.3/8–15) is in effect when the Accumulated Count is equal to or within the values indicated in the Range 2 Starting Value (M0:e.12) and Range 2 Ending Value (M0:e.13).



The Range Starting Value specifies the start of the range and the Range Ending Value specifies the end. While using the Ring Counter Type and the Starting > Ending, the range extends across the rollover count (Maximum Count Value). While using the Linear Counter Type and the Starting > Ending, the range extends from Starting to 32767 and from –32767 to Ending. Refer to the *Range Mode with Linear Counter* example found in chapter 2.

Ranges may overlap. When within more than one range, the outputs of those ranges are combined (logical OR).

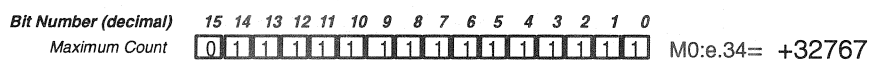
M0:e.34 Maximum Count (Static) / Reset Value (Dynamic)



Maximum Count

When the module is configured as a Ring Counter type, this word allows you to specify the ring rollover count. The range of this value is 1 to +32767. If reset to 0, a configuration error occurs.

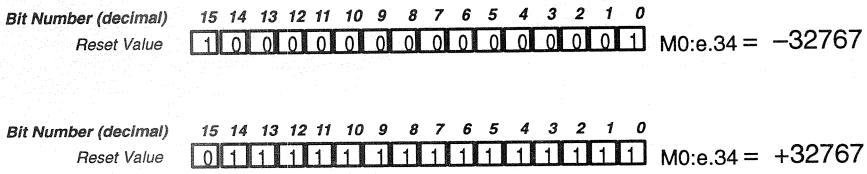
The example below specifies a rollover count of 32,767.



Reset Value

When the module is configured for a linear counter, the counter is reset to the value you enter in this word. This word allows you to initialize the counter, when a reset condition occurs, to a specific value other than zero. The range of this value is –32767 to +32767.

The example below illustrates reset values of –32,767 and +32,767.

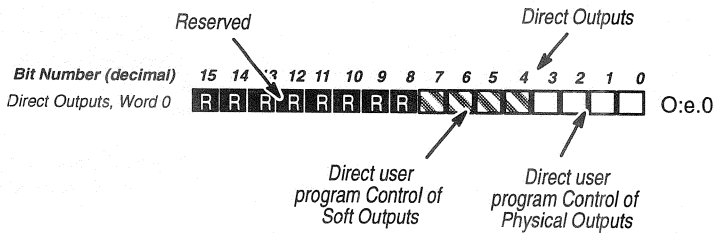


Important: Resetting to a non zero value takes more time than resetting to zero. It is possible to lose counts while a non zero value is being loaded into the counter. Refer to *Timing Information* found in appendix A.

Output Data File Word – Range and Rate Modes

The Output Data File is only one word in size. Appendix E contains worksheets for Range and Rate Mode operation.

O:e.0 Direct Outputs (Dynamic)



O:e.0 Bits 0 through 7 – Direct Outputs

These bits are used for direct user program control of the outputs. Bits 0, 1, 2, and 3 represent the four Physical Outputs of the module. When one of these bits is set, the corresponding output circuit is ON if that output is under user program control (refer to *Output Source Select M0:e.0/0–7*).

Bits 4, 5, 6, and 7 represent Soft Outputs which are not physically connected to output circuits, they are used as system event flags.

Direct Outputs (bits 0–7)	Output Response
0	Corresponding output is OFF
1	Corresponding output is ON

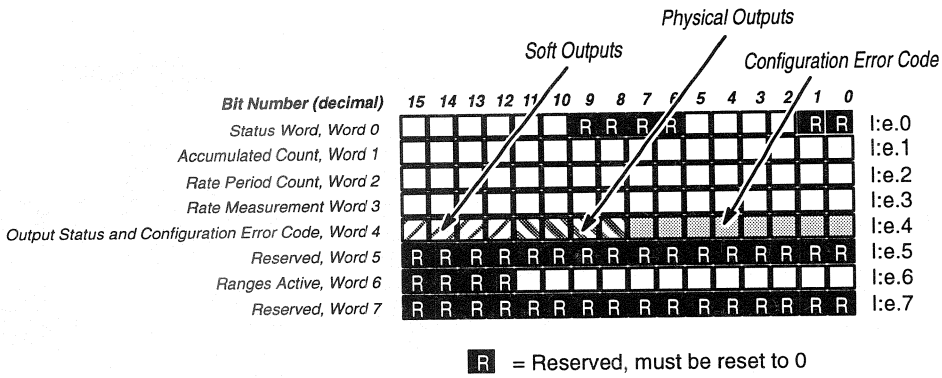
O:e.0 Bits 8 through 15

Bits 8 through 15 are reserved and must be reset to 0.

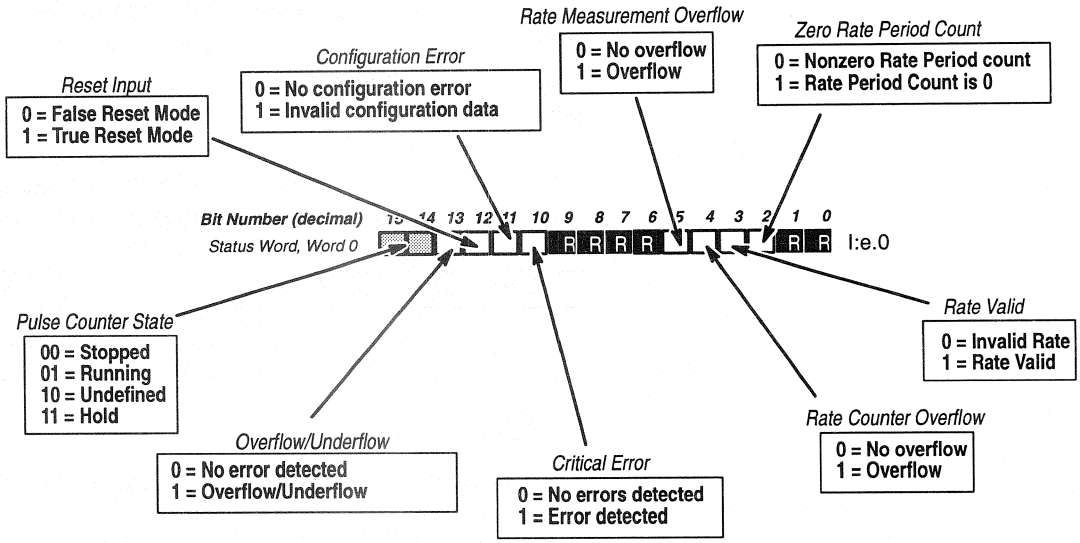
If your user program will not be using the Direct Outputs field, you can improve system throughput by setting the Scanned Output Words to 0.

Input Data File Words – Range and Rate Modes

The figure below shows how the input data file words are used. An explanation of each word follows the figure.



I:e.0 Status Word



I:e.0 Bits 0 and 1

Bits 0 and 1 are reserved and must be reset to 0.

I:e.0 Bit 2 – Zero Rate Period Count

The module sets this bit to 1 whenever the Rate Period Count is found to be zero over a Rate Period.

The bit is cleared to 0:

- any time a non-zero count is obtained
- when there is a Rate Period Count overflow
- upon the 0 to 1 transition of the Function Control bit

Zero Rate Period Count (bit 2)	Cause
0	Non-zero count is obtained, rate period overflow, or, counter function has been enabled
1	Rate Period Count is Zero over a Rate Period

This bit is updated after every Rate Period.

I:e.0 bit 3 – Rate Valid

This bit is cleared upon the 0 to 1 transition of the Function Control bit.

The module sets this bit to 1 when the Rate Measurement and Rate Period Count inputs have valid values that do not cause any overflows. The bit is updated after every Rate Period.

Rate Valid (bit 3)	Condition
0	Rate Measurement and Rate Period Count inputs do not have meaningful data
1	Rate Measurement and Rate Period Count inputs have valid values that do not cause any overflows

I:e.0 bit 4 – Rate Counter Overflow

When this bit is set, a Rate Period Counter overflow has been detected. The bit is dynamically updated after every Rate Period. You can adjust the Rate Period when an overflow is detected. When the overflow occurs, the Rate Period will be set to ±32767. Refer to *Rate Counter Overflow* found in chapter 5.

Rate Counter Overflow (bit 4)	Cause
0	No Rate Period overflow detected
1	Rate Period Counter overflow detected

The module sets this bit to 1 when the Rate Period Counter Overflows. This bit is cleared upon the 0 to 1 transition of the Function Control bit.

I:e.0 Bit 5 – Rate Measurement Overflow

When this bit is set to 1, one of the following conditions exist:

- The calculated Rate Measurement input parameter exceeds the maximum rate of ± 32767 Hz.
- A Rate Period Counter overflow is detected.

The bit is dynamically updated after every Rate Measurement. When the overflow occurs, the Rate Period will be set to ±32767 Hz. The module will continue to run the rate measurement calculation and will clear the error if the input frequency drops below 32767 Hz. If operating in the Rate Mode, the module controlled outputs are reset to 0 while this error is present. Outputs controlled from the user program are not affected.

When a Rate Period does not cause any overflows, the bit is cleared. This bit is cleared upon the 0 to 1 transition of the Function Control bit.

Rate Measurement Overflow (bit 5)	Cause
0	No Rate Period overflow detected
1	Rate Period Counter overflow detected, or maximum rate of ±32767 Hz has been met

I:e.0 Bits 6 through 9

Bits 6 through 9 are reserved and must be reset to 0.

I:e.0 Bit 10 – Critical Error

This bit is set (to 1) by the module whenever a Critical Error is detected. It causes the module operation to halt (even though the Function Control bit is set to 1) and module controlled outputs are turned OFF.

The Critical Errors are:

- Module Configuration Errors (fault LED flashes)
- Linear Counter Overflow/Underflow (fault LED remains off)

For more information, refer to *Error Handling* found on page 5–2.

The error bit is cleared when the Function Control Bit is toggled to 0, then back to 1.

Critical Error (bit 10)	Cause
0	No Critical Error detected
1	Critical Error detected

I:e.0 Bit 11 – Configuration Error

This bit is set to 1 when a configuration error is detected. In addition, the Configuration Error Code bits (I:e.4/0–7) are set.

This bit remains set as long as invalid configuration data exists in the Setup and Control Word (M0:e.1).

Configuration Error (bit 11)	Cause
0	No configuration error detected
1	Configuration error detected

I:e.0 Bit 12 – Reset Input

This bit is set to 1 as long as the condition specified by the Reset Mode (M0:e.1/ 5–7) is true. It is reset while the condition is false.

Reset Input (bit 12)	Reset Mode (M0:e.1/5–7) condition
0	False
1	True

I:e.0 Bit 13 – Overflow/Underflow

When this bit is set, it indicates that the linear counter has overflowed or underflowed. The module controlled outputs are reset to 0 while this error is present.

The bit can be cleared by toggling the Function Control Bit (M0:e.1/12) to 0 and then back to 1. This is a Critical Error.

Overflow/Underflow (bit 13)	Cause
0	No overflow/underflow detected
1	Linear counter has overflowed or underflowed

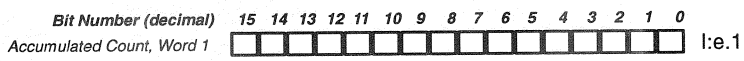
I:e.0 bits 14 and 15 – Pulse Counter State

These bits indicate the current state of the Pulse Counter (the state of the Rate Counter is separate):

Pulse Counter State Bits		Pulse Counter State
15	14	
0	0	stopped
0	1	running
1	0	undefined
1	1	hold

I:e.1 Accumulated Count

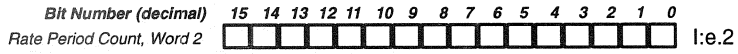
This is the input value from the pulse counter. It gives the total number of counts since the pulse counter was last reset (plus the reset value).



I:e.2 Rate Period Count

The Rate Period Count is generated by the Rate Counter. This word indicates the number of counts obtained during the last Rate Measurement Period.

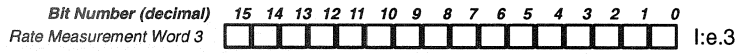
This input value is active in all modes. It is updated along with the Rate Measurement. It will not be scaled down when using the x2 or x4 input type.



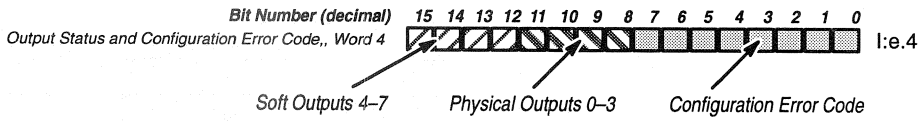
I:e.3 Rate Measurement (Hz)

This word indicates the current rate at which the count is being received (in Hz). This value is updated after every Rate Period.

This input value is active in all modes. When the module is used with encoders and configured for x2 or x4 input types, the calculated value will be scaled down by a factor or two or four respectively.



I:e.4 Output Status, Configuration Error Code



I:e.4 Bits 0 through 7 – Configuration Error Code

Configuration Error Code		Reason	Critical Error	Action
Hex	Binary			
01	0000 0001	not defined	–	reconfigure
02	0000 0010	max count = 0 (ring)	yes	reconfigure
03	0000 0011	invalid operating mode	yes	reconfigure
04	0000 0100	invalid input type	yes	reconfigure
05	0000 0101	static parameter changed	yes	reconfigure
06	0000 0110	ranges active = 0	no	change parameter
07	0000 0111	rate period = 0	no	change parameter
08	0000 1000	linear counter reset value out of range	no	change parameter
09	0000 1001	sequencer preset > max. count	no	change parameter

Reconfigure means the Function Control bit must be reset to 0, the parameter must be changed, and the Function Control bit is then set to 1.

I:e.4 Bits 8 through 15 – Output Status

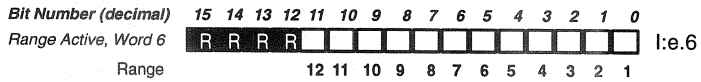
These bits reflect the current state of both the Soft and Physical Outputs. If the Enable Output bit (M0:e.1/1) is false or if the processor is not in run mode, the Physical Outputs are not active.

Bits 8–11 represent the Physical Outputs 0–3. Bits 12–15 represent the Soft Outputs 4–7.

I:e.5 Reserved

I:e.6 Range Active

Bits 0–11 of this word indicate which range, or ranges are currently active. A range is active whenever the current Accumulated Count (I:e.1 for Range Mode) or Rate Measurement (I:e.3 for Rate Mode) is equal to or within the Starting or Ending Value of a range. Whenever this condition is true, the bit associated with the range will be set to 1. For an inactive range, the associated bit is logic 0.



Range Active	Condition
0	range inactive
1	range active

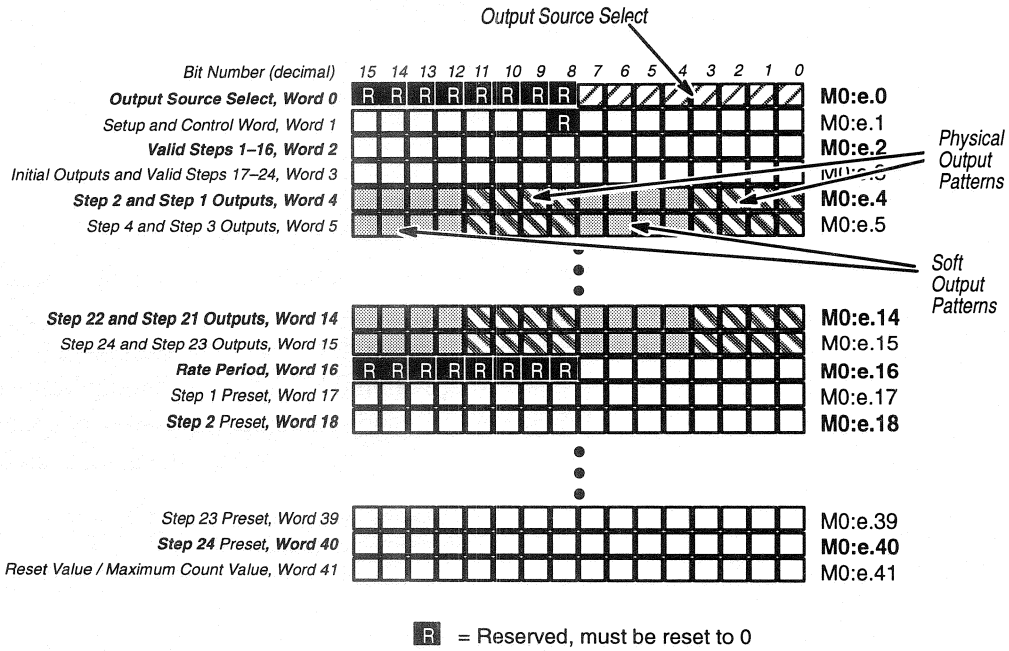
I:e.7 Reserved

M0 File Words – Sequencer Mode

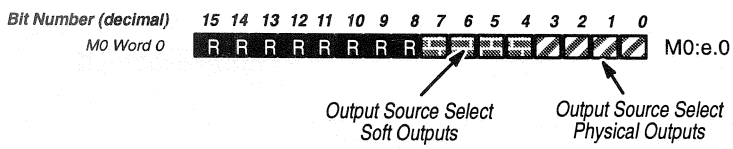
For more information on M0 files, refer to appendix B.

Important: The High-Speed Counter module does not support the interrupt capability described in appendix B.

Appendix F contains worksheets for Sequencer Mode operation.



M0:e.0 Output Source Select



M0:e.0 Bits 0 through 7 – Output Source Select (Dynamic)

Bits 0, 1, 2, and 3 represent the Physical Outputs. Bits 4, 5, 6, and 7 represent the Soft Outputs.

The status of these bits determines whether an output is controlled by the module (when the Function Control bit is set to 1), or by the user program.

Output Source Select (bits 4–7)	Output Status
0	output is under module control
1	output is under user program control

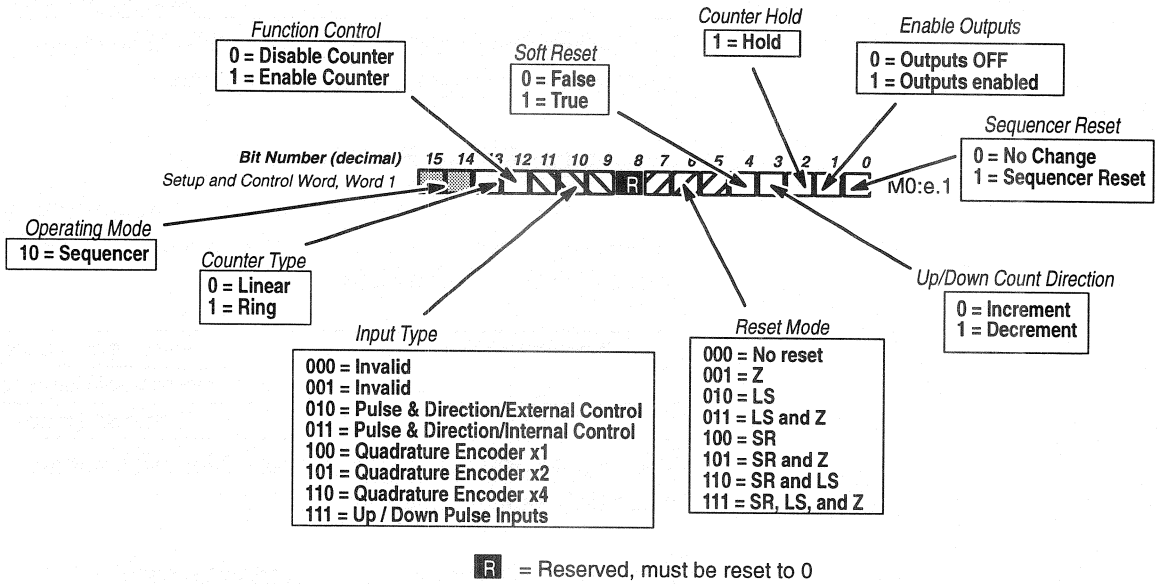
A logic 0 in any of these positions means that the corresponding output is under module control. A logic 1 means that the corresponding output is under user program control (refer to *O:e.0/0–7 Direct Outputs*).

The Output Source Select bit values are dynamic and can be changed by the user program at any time.

M0:e.0 Bits 8 through 15

Bits 8 through 15 are reserved and must be reset to 0.

M0:e.1 Setup and Control Word



M0:e.1 Bit 0 – Sequencer Reset (Dynamic)

This bit determines whether the sequencer is reset each time the counter is reset.

If the pulse counter is reset when this bit is set to 1, the sequencer resets. In addition:

- The Current Sequencer Step (I:e.4/0–7) is reset to zero.
- The Next Sequencer Step Preset (I:e.7) is reset to the preset of the first valid step.
- The Initial Output pattern (M0:e.3/8–15) is sent to the outputs.

When this bit is logic 0 and the pulse counter is reset, the Current Sequencer Step and the output pattern are not affected.

Sequencer Reset (bit 0)	When Counter is Reset
0	no sequencer reset
1	sequencer resets

M0:e.1 Bit 1 – Enable Outputs (Dynamic)

This bit enables the Physical and Soft Outputs (O:e.0/0–7). When the bit is logic 0, outputs are turned off regardless of the state of the module or the Direct Output fields. You must set this bit (to 1) to allow the module to independently control the outputs, or to allow direct output control by the user program.

Enable Outputs (bit 1)	Output Status
0	outputs are OFF
1	outputs are enabled

The Output Source Select field (M0:e.0/0–7) determines whether the module or user program controls the outputs.

M0:e.1 Bit 2 – Counter Hold (Dynamic)

When set to 1, this bit prevents the pulse counter from counting input pulses. In addition, the Pulse Counter State bits in the Status Word (I:e.0/14–15) are set to Hold.

Counter Hold (bit 2)	Pulse Counter State
0	pulses are passed to the pulse counter
1	pulses are ignored

The Counter Reset function and Rate Measurement are not affected when the Counter Hold bit is set.

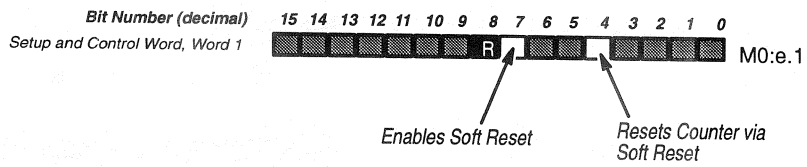
M0:e.1 Bit 3 – Up/Down Count Direction (Dynamic)

This bit allows you to control the direction of the count when the Pulse and Direction with Internal Control Input Type (M0:e.1/9–11) is selected. This bit has no meaning when any other input type is selected.

Up/Down Count Direction (bit 3)	Affect on Accumulated Count
0	accumulated count decrements with each count received in Input A
1	accumulated count increments with each count received in Input A

M0:e.1 Bit 4 – Soft Reset (Dynamic)

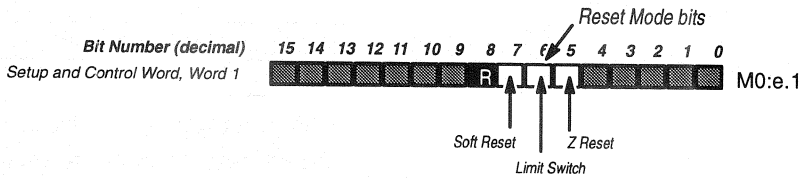
The Soft Reset bit can be used to reset the counter in combination with the physical reset signals. Setting this bit (to 1) resets the counter, via the Reset Mode bits, if Soft Reset (bit 7) is selected. The 0 to 1 transition of the Soft Reset condition (M0:e.1/5–7) resets the counter when configured to do so (refer to *Counter Reset Control* found in chapter 2).



Important: The Soft Reset bit must be held at 1 until the counter resets. The Reset Input bit (I:e.0/12) can be used to detect a counter reset.

M0:e.1 Bits 5,6,7 – Reset Mode (Static)

These bits allow you to select the device(s) that reset the counter. Bit 5 enables the Z reset, Bit 6 enables the limit switch reset, and bit 7 enables the soft reset, as shown below:



Setup and Control Word bits			Reset Condition is True
7	6	5	
0	0	0	Never
0	0	1	When Z is ON
0	1	0	When the limit switch is ON
0	1	1	When the limit switch and Z are ON
1	0	0	When the Soft Reset is 1
1	0	1	When the Soft Reset is 1 and Z is ON
1	1	0	When the Soft Reset is 1 and limit switch is ON
1	1	1	When the Soft Reset is 1, limit switch and Z are ON

You can reset the sequencer to the Initial Output pattern (M0:e.3/8–15) using the Sequencer Reset bit (M0:e.1/0).

The reset of the counter is edge triggered. It occurs only when all of the conditions specified become true. If multiple conditions are selected, the counter is reset on the last event's 0 to 1 transition. For example, if Z and LS are selected (011), Z by itself will not trigger the reset. Z and LS must both be ON.

Important: The time it takes for the counter to reset depends upon the value it resets to. If the reset value is zero, the counter resets immediately on the false to true edge of the reset condition without losing subsequent counts. If the reset value is nonzero, there is a delay of up to 500µs before the reset value is loaded. Count pulses can be lost if they happen during the delay time. Refer to *Timing Information* in appendix A.

M0:e.1 Bit 8

Bit 8 is reserved and must be reset to 0.

M0:e.1 Bits 9,10,11 – Input Type (Static)

You configure this field to define the counter input type you are using:

Setup and Control Word bits			Input Type
11	10	9	
0	0	0	Invalid – configuration error
0	0	1	Invalid – configuration error
0	1	0	Pulse and Direction w/External Control
0	1	1	Pulse and Direction w/Internal Control
1	0	0	Quadrature Encoder Input – X1
1	0	1	Quadrature Encoder Input – X2
1	1	0	Quadrature Encoder Input – X4
1	1	1	Up/Down Pulse Inputs

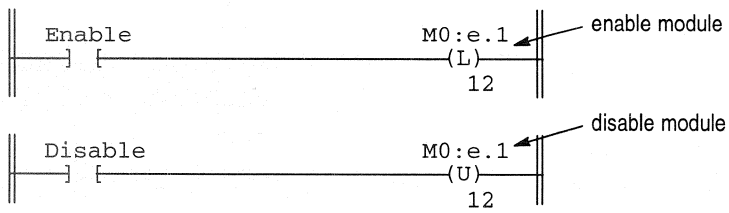
The input type you select determines how the A and B inputs cause the module's counter to increment and decrement. For all three input types, the Z input can be used to force a counter reset. The A, B, and Z inputs operate with input signals up to a maximum rate of 50 KHz.

M0:e.1 Bit 12 – Function Control (Dynamic)

This bit enables and disables the counter function.

Function Control bit	Function
0	Disable counter (except user program controlled outputs)
1	Enable counter

Important: The Function Control Bit must always be controlled by rungs in the ladder logic. Do not set the Function Control bit to 1 until all of your configured parameters are transferred. Never save the program with the Function Control bit set.



Static parameters can be changed when the Function Control Bit equals 0. Module operation will be altered upon the 0 to 1 transition of the Function Control bit.

When the Function Control bit changes from 1 to 0:

1. All outputs under module control are turned off (excluding outputs under user program control).
2. The pulse and rate counters are cleared and held at zero.
3. The following data file fields are cleared:
   - Accumulated Count
   - Rate Period Count, Rate Measurement
   - Sequence Done bit
   - Current Sequence Step
   - Next Sequence Step
   - Output Status
4. The Pulse Counter State field identifies the stopped condition.
5. Configuration errors are cleared.

The user program can change the Function Control bit dynamically in either the run or test modes to reconfigure or control the operation. Note that you can change the preset or range information at any time independent of this bit. Refer to *Timing Information* located in appendix A.

M0:e.1 Bit 13 – Counter Type (Static)

This bit allows you to define the Counter Type:

Counter Type (bit 13)	Counter Type
0	linear
1	ring

M0:e.1 Bits 14 and 15 – Operating Mode (Static)

These bits define the module's Operating Mode:

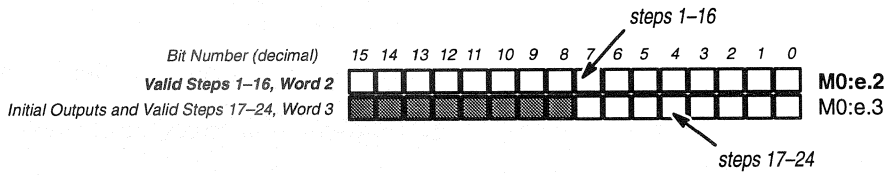
Operating Mode Bits		Operating Mode
15	14	
0	0	invalid
0	1	Range
1	0	Sequencer
1	1	Rate

M0:e.2 and M0:e.3/0–7 Valid Steps (Dynamic)

The Valid Step field determines which steps are enabled. The Sequencer Mode supports 24 steps. You must have at least one Valid Step defined, otherwise the module will fault.

Bits 0 through 15 of word M0:e.2 represent steps 1 through 16 respectively. Bits 0 through 7 of word M0:e.3 represent steps 17 through 24 respectively.

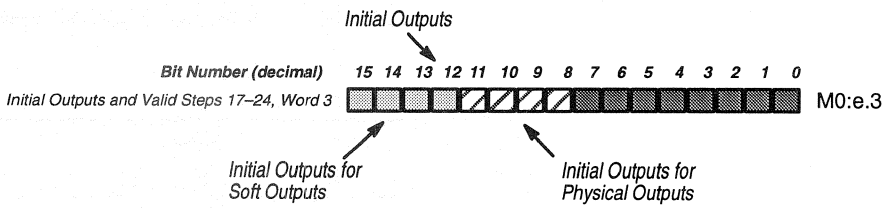
When a bit is set to 1, the corresponding step is enabled. If the bit is reset (to 0), the step is disabled.



Valid Steps for Sequencer Mode	Corresponding Step
0	disabled
1	enabled

M0:e.3 /8–15 Initial Outputs (Dynamic)

The Initial Output is the starting position output pattern. It determines the output pattern until the preset of the first Valid Step is reached.



Repeat Sequence

Preset Number	Desired Trigger	Preset Value	Outputs ① 7	6	5	4	3	2	1	0
	Initial Output		0	0	0	0	0	0	0	0
1	10,000	9,999	0	0	0	0	0	0	0	1
2	20,000	19,999	0	0	0	0	0	0	1	0
3	27,000	26,999	0	0	0	0	0	0	1	1

① Bits 0–3 are Physical Outputs. Bits 4–7 are Set Outputs.

Initial Outputs are applied when the Function Control bit makes a 0 to 1 transition and remains in effect until the first Valid Step is reached. The Initial Output Pattern is not applied again unless:

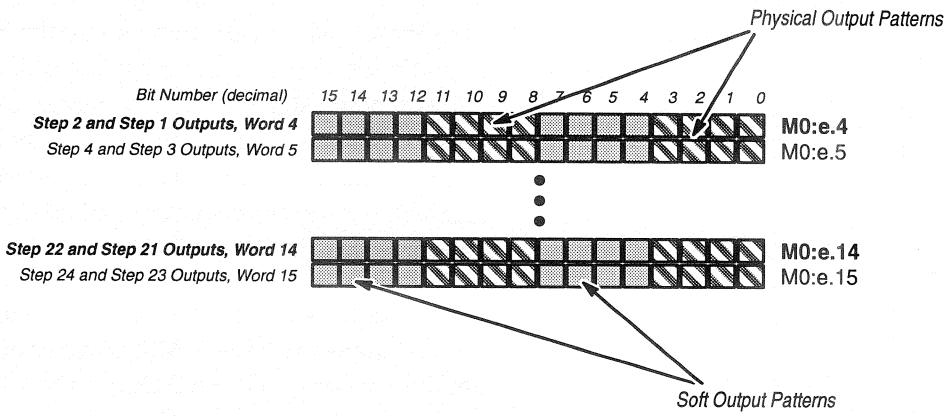
- the Function Control bit makes another 0 to 1 transition
- reset occurs with the Sequencer Reset bit (M0:e.1/0)

M0:e.4 through M0:e.15 – Step 1 through 24 Outputs (Dynamic)

M0:e.4 through M0:e.15 are used to program the specific ON/OFF output patterns for each of the 24 possible steps.

Each output field consists of 8 bits. The four lowest numbered bits correspond to the Physical Outputs of the module; the four highest numbered bits correspond to the Soft Outputs.

For example, in Preset 2 Outputs of word M0:e.4, bits 8, 9, 10, and 11 correspond to the module's Physical Outputs 0, 1, 2, and 3. Bits 12, 13, 14, and 15 correspond to the Soft Outputs.



On the next count after a Step Preset matches the Accumulated Count, the Step Outputs are applied to the output terminal and Output Status field (I:e.4/8–15).

Soft Output bits (I:e.4/8–15) can be used in the user program.

M0:e.16 Rate Period (Dynamic)

M0:e.16 Bits 0 through 16 – Rate Period

The integer value in this word indicates the Rate Period time. The value can range from 1–255. This value is multiplied by 10ms to obtain the actual Rate Period time. For more information, refer to *Selecting the Rate Period Parameter* located in chapter 2.

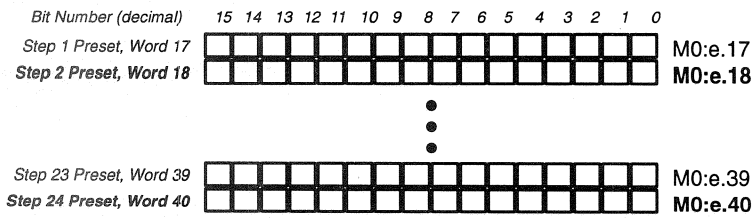
M0:e.16 Bits 8 through 15

Bits 8 through 15 are reserved and must be reset to 0.

M0:e.17 through M0:e.40 Step 1 through 24 Presets (Dynamic)

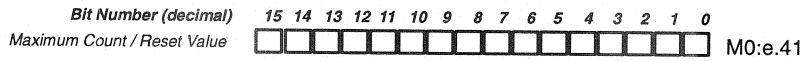
The Sequencer Mode supports 24 steps. Each step has an associated Step Preset. Values are entered into the Step Preset words. The Step 1–24 Preset values define the number of pulses required to reach the corresponding step (the step is reached at one count beyond the preset). This value refers to the Accumulated Count value, not the relative number of pulses received between steps. When a step is reached, the Step Outputs are applied to the output terminals and Output Status field (I:e.4/8–15).

For example, when the Step 2 Preset count (M0:e.18) is reached, the Step 2 Outputs pattern in M0:e.4 takes effect. If you want the output pattern contained in Step 2 Outputs to take effect at count 10000 (and the counter is counting up) – you must set Step 2 Preset to 9999 (because the output pattern becomes valid on the next count after the preset count is reached). The output pattern remains in effect until the next step preset is passed.



Important: The output pattern contained in the Step Output words (M0:e.4–15) takes effect on the next count *after* the Step Preset Value (M0:e.17–40) matches the Accumulated Count.

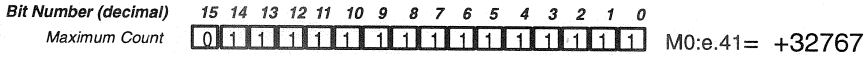
M0:e.41 Maximum Count (Static) / Reset Value (Dynamic)



Maximum Count

When the module is configured as a Ring Counter type, this word allows you to specify the ring rollover count. The range of this value is 1 to +32767. If 0, a configuration error occurs.

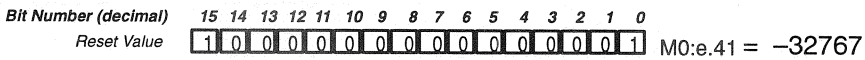
The example below specifies a rollover count of 32,767.

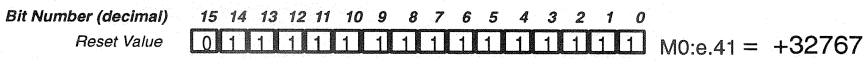


Reset Value

When the module is configured for a linear counter, the counter is reset to the value you enter in this word. This word allows you to initialize the counter, when a reset condition occurs, to a specific value other than zero. The range of this value is –32767 to +32767.

The example below illustrates reset values of –32,767 and +32,767.



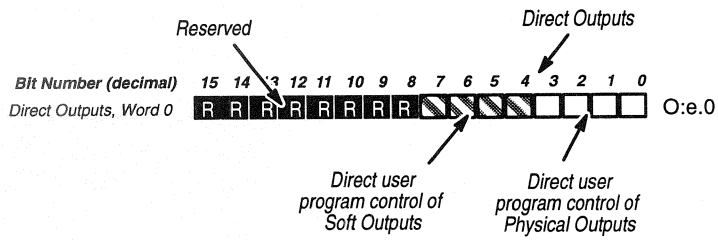


Important: Resetting to a non zero value takes more time than resetting to zero. It is possible to lose counts while a non zero value is being loaded into the counter. Refer to *Timing Information* found in appendix A.

Output Data File Word – Sequencer Mode

The Output Data File is only one word in size. Appendix F contains worksheets for Sequencer Mode operation.

O:e.0 Direct Outputs (Dynamic)



O:e.0 Bits 0 through 7 – Direct Outputs

These bits are used for direct user program control of the outputs. Bits 0, 1, 2, and 3 represent the four Physical Outputs of the module. When one of these bits is set, the corresponding output circuit is ON if that output is under user program control (refer to *Output Source Select M0:e.0/0–7*).

Bits 4, 5, 6, and 7 represent Soft Outputs which are not physically connected to output circuits, but are the same in all other respects.

Direct Outputs (bits 0–7)	Output Response
0	Corresponding output is OFF
1	Corresponding output is ON

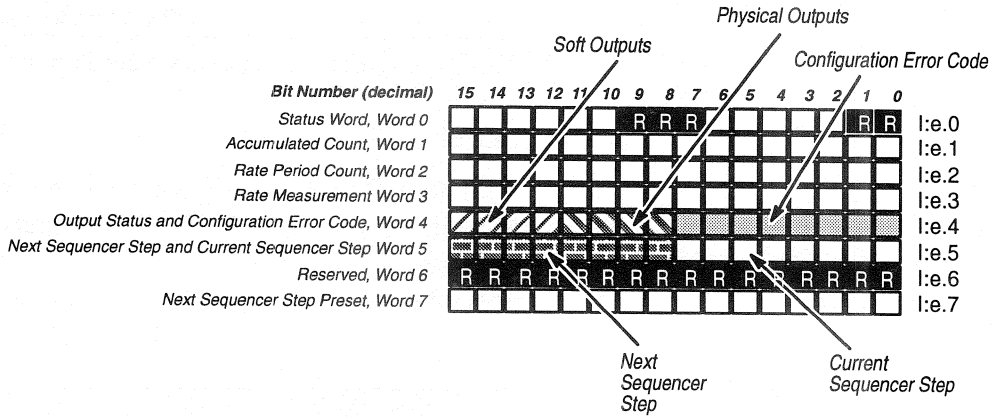
O:e.0 Bits 8 through 15

Bits 8 through 15 are reserved and must be reset to 0.

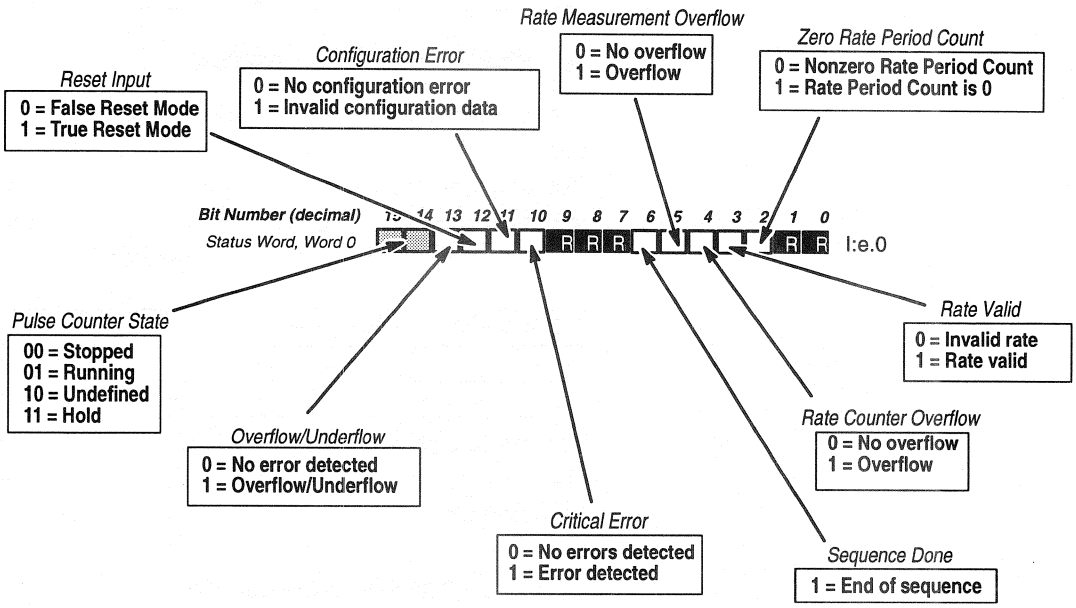
If your user program will not be using the Direct Outputs field, you can improve system throughput by setting the Scanned Output Words to 0.

Input Data File Words – Sequencer Mode

The figure below shows how the input data file words are used. An explanation of each word follows the figure.



I:e.0 Status Word



I:e.0 Bits 0 and 1

Bits 0 and 1 are reserved and must be reset to 0.

I:e.0 Bit 2 – Zero Rate Period Count

The module sets this bit to 1 whenever the Rate Period Count is found to be zero over a Rate Period.

The bit is cleared to 0:

- any time a non-zero count is obtained
- when there is a Rate Period Count overflow
- upon the 0 to 1 transition of the Function Control bit

Zero Rate Period Count (bit 2)	Cause
0	Non-zero count is obtained, rate period overflow, or, counter function has been enabled
1	Rate period count is zero over a rate period

This bit is updated after every Rate Period.

I:e.0 Bit 3 – Rate Valid

I:e.0 bit 3, Rate Valid – The module sets this bit to 1 when the Rate Measurement and Rate Period Count inputs have valid values that do not cause any overflows. The bit is updated after every Rate Period. This bit is cleared upon the 0 to 1 transition of the Function Control bit.

Rate Valid (bit 3)	Condition
0	Rate Measurement and Rate Period Count inputs do not have meaningful data
1	Rate Measurement and Rate Period Count inputs have valid values that do not cause any overflows

I:e.0 Bit 4 – Rate Counter Overflow

When this bit is set, a Rate Period Counter overflow has been detected. The bit is dynamically updated after every Rate Period. You can adjust the Rate Period when an overflow is detected. When the overflow occurs, the Rate Period will be set to ±32767. Refer to *Rate Counter Overflow* found in chapter 5.

Rate Counter Overflow (bit 4)	Cause
0	No rate period overflow detected
1	Rate period counter overflow detected

The module sets this bit to 1 when the Rate Period Counter Overflows. This bit is cleared upon the 0 to 1 transition of the Function Control bit.

I:e.0 Bit 5 – Rate Measure Overflow

When this bit is set to 1, one of the following conditions exist:

- The calculated Rate Measurement input parameter exceeds the maximum rate of ± 32767.
- A Rate Period Counter overflow is detected.

The bit is dynamically updated after every Rate Measurement. When the overflow occurs, the Rate Period will be set to ±32767 Hz.

When a Rate Period does not cause any overflows, the bit is cleared. This bit is cleared upon the 0 to 1 transition of the Function Control bit.

Rate Measurement Overflow (bit5)	Cause
0	No rate period overflow detected
1	Rate period counter overflow detected, or maximum rate of ±32767 Hz has been met

I:e.0 Bit 6 – Sequence Done

This bit is set whenever the end of sequence is reached. This bit is set (and remains set) as long as the last preset output data is in effect. This bit is cleared when the last preset output data is not in effect.

Sequence Done (bit6)	Cause
0	preset is valid
1	end of sequence

I:e.0 Bits 7,8,9

Bits 7, 8, and 9 are reserved and must be reset to 0.

I:e.0 Bit 10 – Critical Error

This bit is set (to 1) whenever a Critical Error is detected that causes the module operation to halt (even though the Function Control Bit is set to 1) and module controlled outputs are turned OFF.

The errors are:

- Module Configuration Errors (fault LED flashes)
- Linear Counter Overflow/Underflow (fault LED remains off)

The error bit is cleared when the Function Control Bit is toggled to 0, then back to 1.

Critical Error (bit10)	Cause
0	no critical error detected
1	critical error detected

I:e.0 Bit 11 – Configuration Error

This bit is set to 1 when a configuration error is detected. In addition, the Configuration Error Code bits (I:e.4/0–7) are set.

This bit remains set as long as invalid configuration data exists in the Setup and Control Word (M0:e.1).

Configuration Error (bit 11)	Cause
0	no configuration error detected
1	configuration error detected

I:e.0 Bit 12 – Reset Input

This bit is set to 1 as long as the condition specified by the Reset Mode (M0:e.1/ 5–7) is true. It is reset while the condition is false.

Reset Input (bit 12)	Reset Mode (M0:e.1/5–7) Condition
0	false
1	true

I:e.0 Bit 13 – Overflow/Underflow

When this bit is set, it indicates that the linear counter has overflowed or underflowed. The module controlled outputs are reset to 0 while this error is present.

The bit can be cleared by toggling the Function Control Bit (M0:e.1/12) to 0 and then back to 1. This is a Critical Error.

Overflow/Underflow (bit 13)	Cause
0	no overflow/underflow detected
1	linear counter has overflowed or underflowed

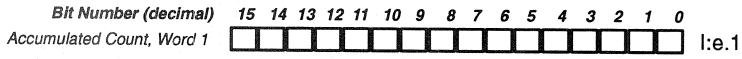
I:e.0 Bits 14 and 15 – Pulse Counter State

These bits indicate the current state of the Pulse Counter (the state of the Rate Counter is separate):

Pulse Counter State Bits		Pulse Counter State
15	14	
0	0	stopped
0	1	running
1	0	undefined
1	1	hold

I:e.1 Accumulated Count

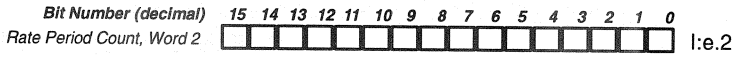
This is the input value from the pulse counter. It gives the total number of counts since the pulse counter was last reset (plus the reset value).



I:e.2 Rate Period Count

This word indicates the number of counts obtained during the last Rate Measurement Period.

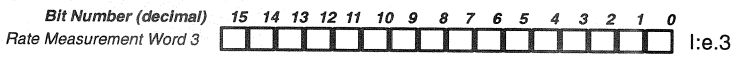
This input value is active in all modes. It is updated along with the Rate Measurement. It will not be scaled down when using the x2 or x4 input type.



I:e.3 Rate Measurement (Hz)

This word indicates the current rate at which the count is being received (in Hz). This value is updated after every Rate Period.

This input value is active in all modes. When the module is used with encoders and configured for x2 or x4 input types, the calculated value will be scaled down by a factor or two or four respectively.



I:e.4 Output Status, Configuration Error Code

I:e.4 Bits 0 through 7 – Configuration Error Code

Configuration Error Code		Reason	Critical Error	Action
Hex	Binary			
01	0000 0001	not defined	–	reconfigure
02	0000 0010	max count = 0 (ring)	yes	reconfigure
03	0000 0011	invalid operating mode	yes	reconfigure
04	0000 0100	invalid input type	yes	reconfigure
05	0000 0101	static parameter changed	yes	reconfigure
06	0000 0110	ranges active = 0	no	change parameter
07	0000 0111	rate period = 0	no	change parameter
08	0000 1000	linear counter reset value out of range	no	change parameter
09	0000 1001	sequencer preset > max. count	no	change parameter

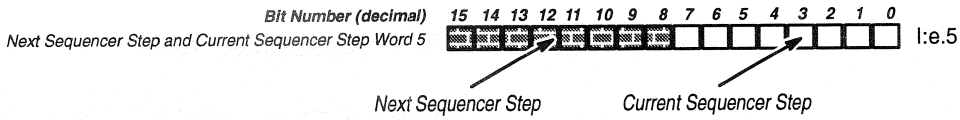
Reconfigure means the Function Control bit must be reset to 0, the parameter must be changed, and the Function Control bit is then set to 1.

I:e.4 Bits 8 through 15 – Output Status

These bits reflect the current state of both the Soft and Physical Outputs. If the Enable Output bit (M0:e.1/1) is false or if the processor is not in run mode, the Physical Outputs are not active.

Bits 8–11 represent the Physical Outputs 0–3. Bits 12–15 represent the Soft Outputs 4–7.

I:e.5 Next Sequencer Step, Current Sequencer Step



I:e.5 Bits 0 through 7 – Current Sequencer Step

These bits indicate the actual step position currently in effect. This parameter is valid only when the Sequencer Mode is in effect. The module outputs under module control will correspond to the current step number.

For example, if the sequencer has reached step is 2, the Step 2 Outputs are active and shown in the Output Status field (I:e.4/8–15)

I:e.5 Bits 8 through 15 – Next Sequencer Step

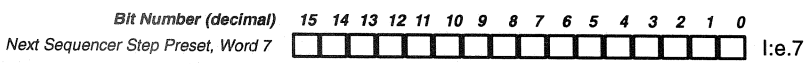
The next valid sequencer step appears here. This parameter is only valid when the module is in the Sequencer Mode. After the Next Sequencer Step Preset is reached, this field is updated to the next valid step in the sequence. If the end of the sequence was reached, this value will be updated to the first valid step after step 0. If no valid steps are found, a configuration error is generated.

The Next Sequencer Step corresponds to the next valid step. For example, If step 1 has been reached and steps 2 through 4 are disabled, 5 is the next valid step.

I:e.6 Reserved

I:e.7 Next Sequencer Step Preset

This word indicates the next step preset value. When the pulse counter passes this value, the sequencer advances to the Next Sequencer Step.



Start Up, Operation and Troubleshooting

This chapter provides start up, operation, troubleshooting, and error handling information.

Start Up

The following steps will assist you in the start up of your module.

1. Install the module in your SLC chassis.
2. Wire the input and output devices as discussed in chapter 3.
3. Configure and program your SLC processor to operate with the module as discussed in chapter 4.
4. Apply power to the SLC system and the attached input and output devices.

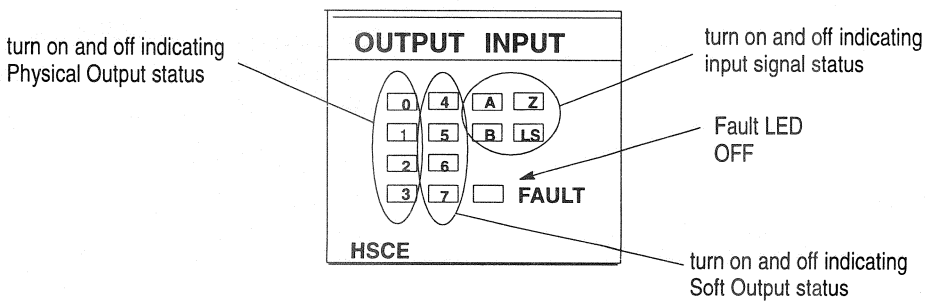
When power is applied to the SLC system, the SLC processor and module run through a power up diagnostic sequence. After the diagnostics are successfully completed, the SLC processor enters run mode and normal operation begins.

If the SLC processor was in the program (or test) mode when power was removed, it will return to the program (or test) mode when power is reapplied. Place the SLC processor into run mode using an SLC programming device.

Normal Operation

During normal operation, the LEDs are illuminated as follows:

- The FAULT LED will be off.
- LEDs A, B, Z, and LS illuminate indicating the input is energized.
- LEDs 0, 1, 2, and 3 illuminate indicating the Physical Output status.
- LEDs 4, 5, 6, and 7 illuminate indicating the Soft Output status.



Troubleshooting

The key tools in diagnosing problems are:

- module LEDs
- SLC processor CPU fault LED
- SLC processor fault code (S:6)
- Status Word in the module's Input Data File (I:e.0)
- Configuration Error Code in the module's Input Data File (I:e.4/0–3)

The following table will help in isolating problems:

CPU FAULT LED (SLC Processor)	FAULT LED (module)	Status Word I:e.0 (module)	Problem	Action
flashing red	off	–	SLC system fault	Refer to *SLC System Fault.*
flashing red	solid red	–	Module diagnostic error	Cycle power. If condition persists, replace the module. Refer to *Module Diagnostic Errors.*
off	flashing red	–	Module configuration error	Refer to *Module Configuration Errors.*
off	off	bit 13 set	Linear counter overflow	Reconfigure module and restart operation. Refer to *Application Errors.*
off	off	bit 5 set	Rate Counter or Rate Measurement Overflow	Change rate period or lower input rate. Refer to *Application Errors.*
off	off	–	Counter value does not change	Refer to *Application Errors.*

Error Handling

In addition to the SLC processor system fault, the following three module generated errors can occur:

- Module Diagnostic errors
- Module Configuration Errors
- Application Errors

SLC System Fault

If a fault has occurred in the SLC system and the SLC fault code indicates the slot the module is installed in, it might be associated with the module I/O configuration. Refer to the following table.

SLC Fault Code (S:6)	Possible Reason
xx54①	Wrong ID Code was entered
xx55①	Wrong ID Code was entered or wrong input and output size was entered
xx5C①	Wrong M0 or M1 file size was entered

① "xx" refers to the slot where the module is installed.

Module Diagnostic Errors

A module diagnostic error is produced if the power up self–test or run–time–watchdog tests fail. This is an indication of a potential hardware failure on the module.

In response to a diagnostic error all module operations are halted, the outputs are reset to 0, and a fault indication is sent to the SLC processor. The module Fault LED is turned on solid red.

Module Configuration Errors

A configuration error is caused by improper set up of a module parameter when the Function Control bit is set (to 1) or by a dynamic parameter that is changed to an improper value. The module responds to a configuration error by flashing the module Fault LED and setting the Configuration Error bit (I:e.0/11) to 1.

The parameter that caused the error is indicated in the Configuration Error Code field (I:e.4/0–7). The table below lists the configuration error code and indicates the required action to clear the error.

Configuration Error Code		Reason	Critical Error	Action
Hex	Binary			
01	0000 0001	not defined	–	reconfigure
02	0000 0010	max count = 0 (ring)	yes	reconfigure
03	0000 0011	invalid operating mode	yes	reconfigure
04	0000 0100	invalid input type	yes	reconfigure
05	0000 0101	static parameter changed	yes	reconfigure
06	0000 0110	ranges active = 0	no	change parameter
07	0000 0111	rate period = 0	no	change parameter
08	0000 1000	linear counter reset value out of range	no	change parameter
09	0000 1001	sequencer preset > max. count	no	change parameter

Reconfigure means that the Function Control bit must be reset to 0, the parameter must be changed, and the Function Control bit then set to 1.

Application Errors

The module can encounter the following application errors.

Linear Counter Overflow/Underflow

When the maximum count is exceeded, the Over/Underflow bit (I:e.0/13) is set to 1. Clearing this error requires reconfiguration. The module controlled outputs are reset to 0 while this error is present. Outputs controlled by the user program are not affected.

Rate Counter Overflow

When the Rate Counter exceeds 32,767, the Rate Counter Overflow bit (I:e.0/4) is set to 1. The module will continue to run the rate measurement and will clear this error if the input frequency drops enough to avoid the counter overflow.

This error can also be cleared by the user program reducing the Rate Period parameter. If operating in the Rate Mode, the module controlled outputs are reset to 0 while this error is present. Outputs controlled from the user program are not affected.

Important: When this bit is set, the Rate Measurement Overflow bit (I:e.0/5) is set.

Rate Measurement Overflow

When the Rate Measurement exceeds 32,767 Hz, the Rate Measurement overflow bit (I:e.0/5) is set to 1. The module will continue to run the rate measurement calculation and will clear the error if the input frequency drops below 32,767 Hz. If operating in the Rate Mode, the module controlled outputs are reset to 0 while this error is present. Outputs controlled from the user program are not affected.

Counter Value Does Not Change

Check the module LEDs for channel A and B inputs with pulses coming in. The A and B LEDs should illuminate regardless of the software configuration of the High–Speed Counter module.

If the A and B LEDs are *not* illuminated, check the power to the input sensor, and the wiring from the sensor to the module.

If the A and B LEDs are illuminated, make sure that configuration of the module is complete and that the Function Control bit has been set to 1 by your program. Also make sure the Counter Hold bit has *not* been set.

If input channel will not turn off, check the leakage current of the input sensor (refer to *Max Off–state Leakage Current* located in appendix A).

Counter Value/Rate Goes in the Wrong Direction

If differential quadrature encoder inputs are used, swap channels A and B to change the direction.

If *pulse and direction inputs are used*, check the Direction and Input Type (M0:e.1/3 and M0:e.1/9–11).

If using up/down count mode, make sure Inputs A and B have not been switched.

Output Does Not Come On

Make sure SLC processor is in run mode.

Check the associated module LED for the output.

- If the LED is illuminated check the power supply and its connections to the module. Also check the connections to the output device.
- If the LED is *not* illuminated make sure the SLC processor is in run mode and that a module fault has not occurred. Check the Output Status field of the input image (I:e.4/8–15) to see if the module is trying to energize the output. If not, make sure the Function Control bit (M0:e.1/12) and Enable Output bit (M0:e.1/1) are set to 1. Make sure the Output Selection field (M0:e.0/0–7) is properly set up.

Output Does Not Turn Off

Check the associated module LED for the output.

- If the LED is illuminated, check your program operation.
- If the LED is *not* illuminated, check the wiring to your output device. Check the leakage current of your connected device (for more information, refer to appendix A).

Application Examples

This chapter contains the following application examples:

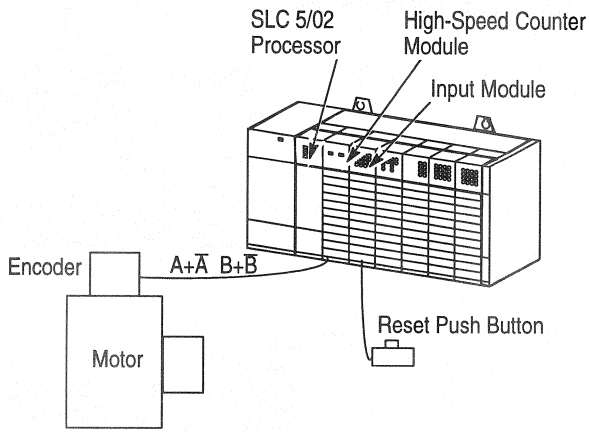
- a basic count-only example using the Rate Mode
- supplementary examples that represent the Range, Rate, and Sequencer Modes

Important: Appendixes E and F contain blank worksheets to assist you when configuring your module. Appendix E contains worksheets for Range and Rate Mode operation. Appendix F contains worksheets for the Sequencer Mode operation.

Basic Count-Only Example

This basic example is provided to get you started using the High-Speed Counter module. This Count-Only example demonstrates how to configure your module to read the number of accumulated pulses from an encoder or other high-speed device, and apply this information to your ladder program. See appendix A for timing information.

Configure slot 1 for the High-Speed Counter module and slot 2 for an input module as shown below.



The following is a brief description of the application.

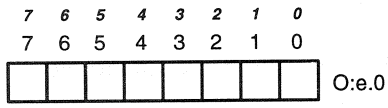
1. The processor monitors the number of pulses that the module has counted. If this number is greater than or equal to 2500, bit B3/0 is energized. If this number is less than 2500, bit B3/1 is energized.
2. If the count reaches 30,000 the accumulator of the module resets to zero automatically.

3. If you press the Reset Push Button, the accumulator of the module is reset, regardless of the current count. (Pressing the Reset Push Button causes the module's soft reset bit to latch and remain latched until the module acknowledges the reset by setting the Input Reset bit.)

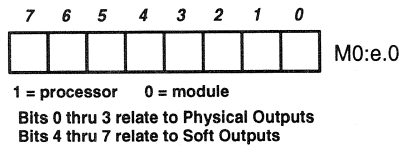
Configuration Worksheets

Shown below is the Range/Rate Mode Configuration Worksheet for M0 Files. A blank worksheet is supplied in appendix E. For the Count-Only example, place the M0 configuration for the module in data N10.

Direct Outputs (page 4–15)

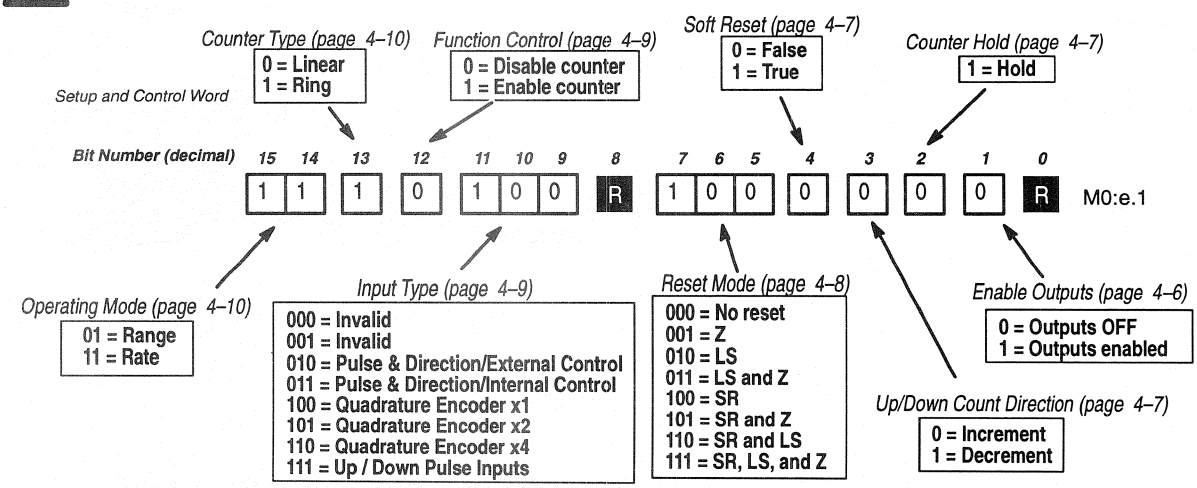


Output Source Select (page 4–5)



Setup and Control Word (page 4–6)

ATTENTION: The module will fault on power-up if you do not enter a value.



Valid Ranges (page 4–11)

ATTENTION: The module will fault on power-up if you do not enter a value.

Bit Number (decimal)	15	14	13	12
Range Number				
Valid Range	R	R	R	R

11	10	9	8	7	6	5	4	3	2	1	0
12	11	10	9	8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0	0	0	1

M0:e.2

1 = range is valid. At least one range must be valid.

Range Outputs (page 4–11)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Number	7	6	5	4	3	2	1	0
Range 2 Outputs								
Range 4 Outputs								
Range 6 Outputs								
Range 8 Outputs								
Range 10 Outputs								
Range 12 Outputs								

7	6	5	4	3	2	1	0	
7	6	5	4	3	2	1	0	
Range 1 Outputs								M0:e.3
Range 3 Outputs								M0:e.4
Range 5 Outputs								M0:e.5
Range 7 Outputs								M0:e.6
Range 9 Outputs								M0:e.7
Range 11 Outputs								M0:e.8

Rate Period (decimal) (page 4–12)

ATTENTION: The module will fault on power-up if you do not enter a value.

Rate Period	1	0	0	M0:e.9

1 to 255 = 10 ms to 2.55 seconds

R = Reserved, must be reset to 0

Starting and Ending Range Values (decimal) (page 4–12)

Range 1 Starting Value		**M0:e.10**
Range 1 Ending Value		M0:e.11
Range 2 Starting Value		**M0:e.12**
Range 2 Ending Value		M0:e.13
Range 3 Starting Value		**M0:e.14**
Range 3 Ending Value		M0:e.15
Range 4 Starting Value		**M0:e.16**
Range 4 Ending Value		M0:e.17
Range 5 Starting Value		**M0:e.18**
Range 5 Ending Value		M0:e.19
Range 6 Starting Value		**M0:e.20**
Range 6 Ending Value		M0:e.21
Range 7 Starting Value		**M0:e.22**
Range 7 Ending Value		M0:e.23
Range 8 Starting Value		**M0:e.24**
Range 8 Ending Value		M0:e25
Range 9 Starting Value		**M0:e.26**
Range 9 Ending Value		M0:e.27
Range 10 Starting Value		**M0:e.28**
Range 10 Ending Value		M0:e.29
Range 11 Starting Value		**M0:e.30**
Range 11 Ending Value		M0:e.31
Range 12 Starting Value		**M0:e.32**
Range 12 Ending Value		M0:e.33

Reset Value/Maximum Count Value (page 4–13)

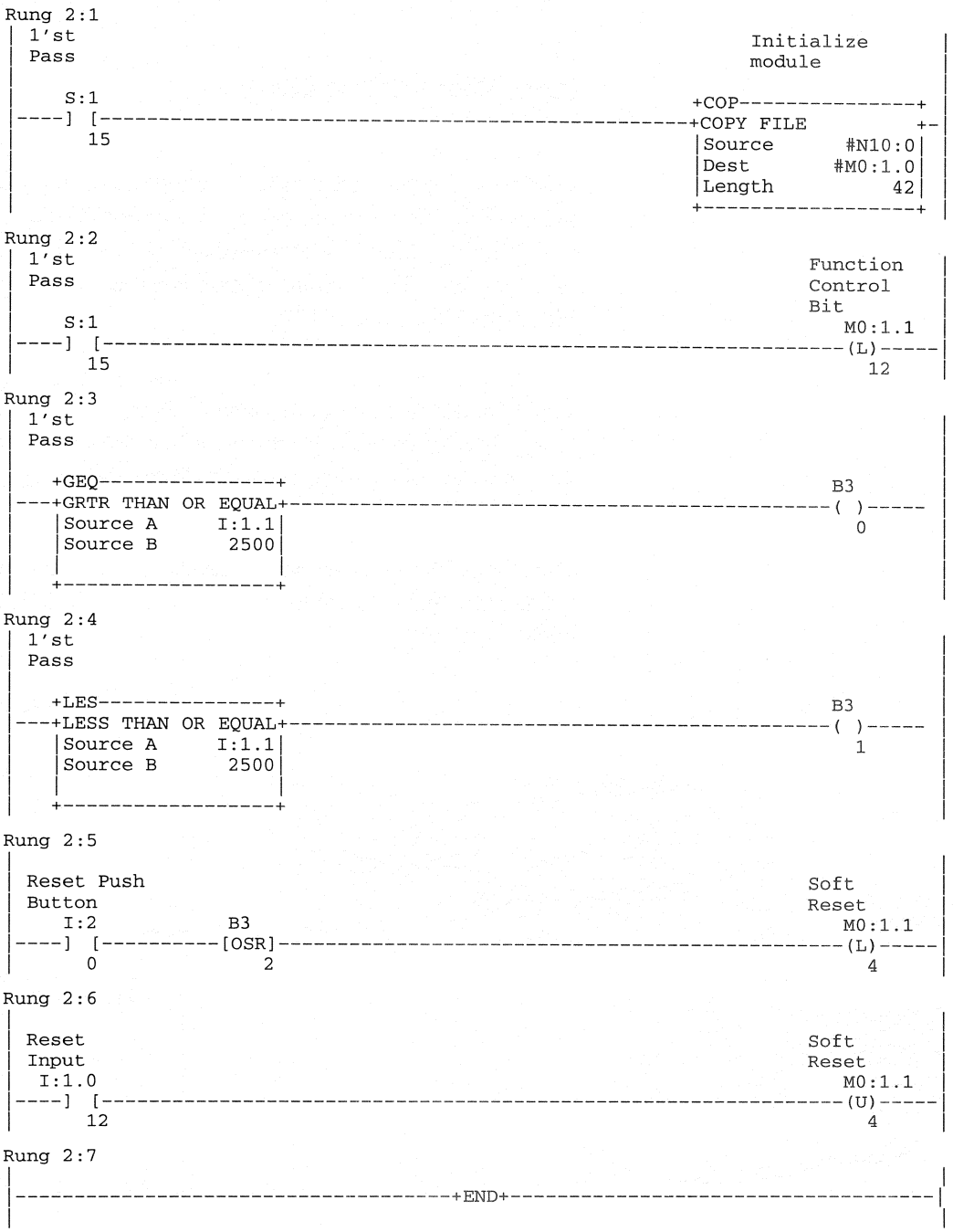
ATTENTION: The module will fault on power-up if you do not enter a value.

Reset Value/Maximum Count Value	3 0 0 0 0	M0:e.34

Ring counter – Maximum Count Value range is 1 to 32767 (rollover at +32767)
Linear counter – Reset Value range is –32767 to +32767.

User Program

Shown below is the user program for the Count-Only example.



Supplementary Examples

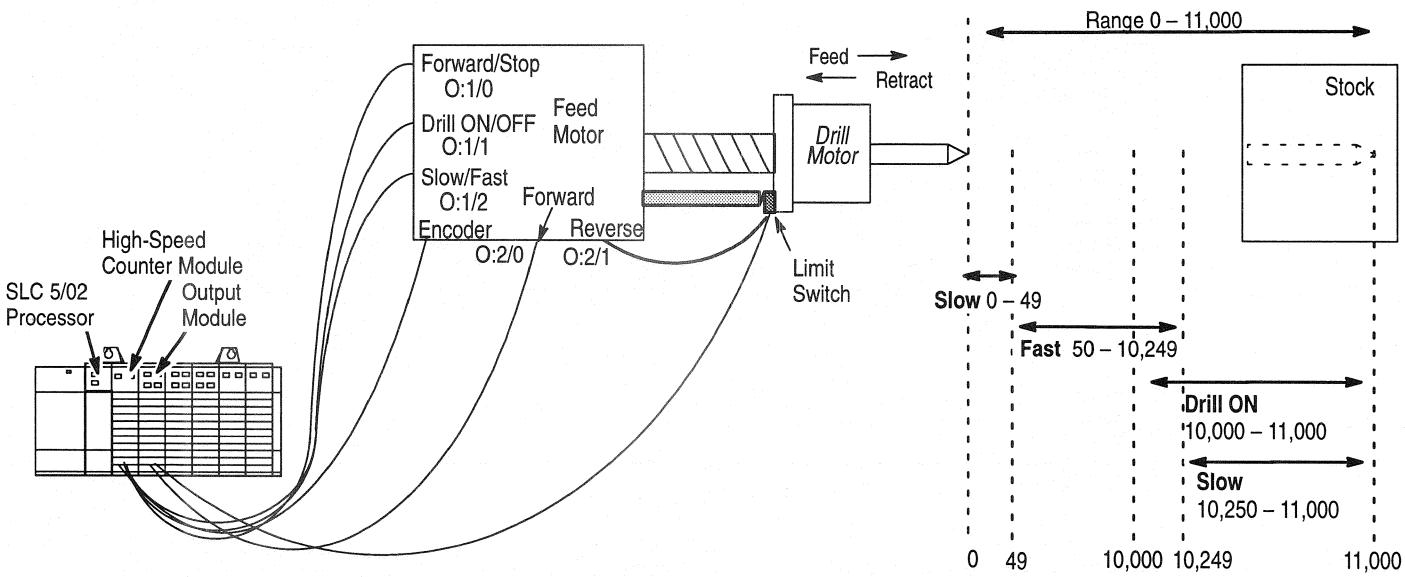
This section contains three application examples that represent the Range, Rate, and Sequencer Modes. Each example has a description, timing information, and configuration worksheets. Additional worksheets are contained in appendixes E and F.

Range Mode – Drilling Example

In this example a hole is drilled into a piece of stock. The drill bit is spun by a single speed, single direction motor that is controlled by the module. The feed motor has two speeds (fast and slow) and travels in two directions (forward and reverse), it is controlled by the user program. The forward motion is halted by energizing Forward Stop (module output O:1/0).

The encoder (not shown) is connected directly to the feed motor shaft. The Pulse Counter increments as the drill travels in the forward direction and decrements as the drill travels in the reverse direction. A limit switch is used to home the feed motor position when retracted.

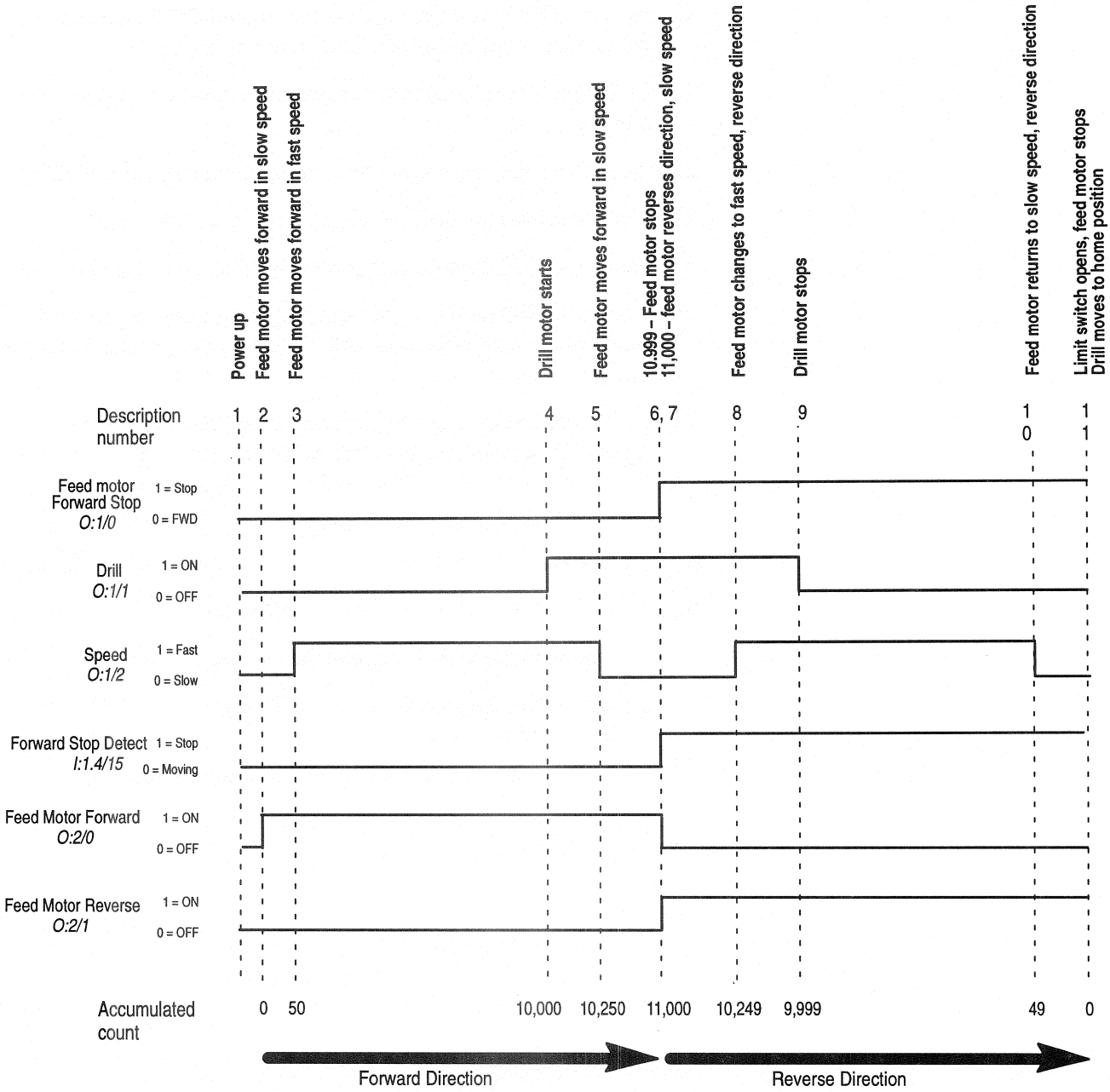
The Range Mode is used in this example because you can easily change the ranges to compensate for changes in hole depth and/or thickness of stock.



The following is a brief description of the application.

1. The drill (O:1/1) and feed motors (O:2/0 and O:2/1) are off. The drill is in the home position (limit switch is open).
2. The feed motor (O:2/0) moves forward in the slow speed until count 49.
3. At count 50, the drill moves forward in the fast speed (O:1/2).
4. At count 10,000 the drill bit begins turning (O:1/1).
5. At count 10,250 the feed motor returns to the slow speed (O:1/2).
6. At count 10,999 the Forward Stop output disables the forward motion of the feed motor. (O:2/0). The drill motor (O:1/1) is still turning.
7. The Forward Stop range begins at count 11,000. The user program detects that the Forward Stop range has been entered using Soft Output bit 7① The feed motor returns to the slow speed (O:1/2), reverse direction (O:2/1).
8. At 10,249 counts, the feed motor enters the fast speed (O:1/2).
9. At count 9,999, the drill motor turns off (O:1/1).
10. At count 49 the feed motor enters the slow speed (O:1/2).
11. At count 0 the limit switch opens, the feed motor (O:2/1) stops, and the drill moves to its home position.

① The Soft Output is set using the Output Data File (O:1/7) and is monitored in the Output Status field (I:1.4/15).


Power up
Feed motor moves forward in slow speed
Feed motor moves forward in fast speed
Drill motor starts
Feed motor moves forward in slow speed
10,999 – Feed motor stops
11,000 – feed motor reverses direction, slow speed
Feed motor changes to fast speed, reverse direction
Drill motor stops
Feed motor returns to slow speed, reverse direction
Limit switch opens, feed motor stops
Drill moves to home position
Description number
1 2 3 4 5 6, 7 8 9 10 11
Feed motor Forward Stop O:1/0
1 = Stop
0 = FWD
Drill O:1/1
1 = ON
0 = OFF
Speed O:1/2
1 = Fast
0 = Slow
Forward Stop Detect I:1.4/15
1 = Stop
0 = Moving
Feed Motor Forward O:2/0
1 = ON
0 = OFF
Feed Motor Reverse O:2/1
1 = ON
0 = OFF
Accumulated count
0 50 10,000 10,250 11,000 10,249 9,999 49 0
Forward Direction
Reverse Direction

Configuration Worksheets

Shown below is the Range/Rate Mode Configuration Worksheet. A blank worksheet is supplied in appendix E.

Direct Outputs (page 4–15)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Number								
Direct Outputs	R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	O:e.0

1 = output ON if under processor control
Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

Output Source Select (page 4–5)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Source Select	R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	M0:e.0

1 = processor 0 = module
Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

Setup and Control Word (page 4–6)

ATTENTION: The module will fault on power-up if you do not enter a value.

Setup and Control Word

Bit Number (decimal)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	0	1	0	0	1	0	0	R	1	0	0	0	0	0	1	R	M0:e.1

- Counter Type (page 4–10): 0 = Linear, 1 = Ring
- Function Control (page 4–9): 0 = Disable counter, 1 = Enable counter
- Soft Reset (page 4–7): 0 = False, 1 = True
- Counter Hold (page 4–7): 1 = Hold
- Operating Mode (page 4–10): 01 = Range, 11 = Rate
- Input Type (page 4–9): 000 = Invalid; 001 = Invalid; 010 = Pulse & Direction/External Control; 011 = Pulse & Direction/Internal Control; 100 = Quadrature Encoder x1; 101 = Quadrature Encoder x2; 110 = Quadrature Encoder x4; 111 = Up / Down Pulse Inputs
- Reset Mode (page 4–8): 000 = No reset; 001 = Z; 010 = LS; 011 = LS and Z; 100 = SR; 101 = SR and Z; 110 = SR and LS; 111 = SR, LS, and Z
- Enable Outputs (page 4–6): 0 = Outputs OFF, 1 = Outputs enabled
- Up/Down Count Direction (page 4–7): 0 = Increment, 1 = Decrement

Valid Ranges (page 4–11)

ATTENTION: The module will fault on power-up if you do not enter a value.

Bit Number (decimal)	15	14	13	12
Range Number				
Valid Range	R	R	R	R

11	10	9	8	7	6	5	4	3	2	1	0	
12	11	10	9	8	7	6	5	4	3	2	1	
0	0	0	0	0	0	0	1	1	1	1	1	M0:e.2

1 = range is valid. At least one range must be valid.

Range Outputs (page 4–11)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Number	7	6	5	4	3	2	1	0
Range 2 Outputs	0	0	0	0	0	1	0	0
Range 4 Outputs	0	0	0	0	0	0	1	0
Range 6 Outputs								
Range 8 Outputs								
Range 10 Outputs								
Range 12 Outputs								

7	6	5	4	3	2	1	0	
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	M0:e.3
0	0	0	0	0	0	0	0	M0:e.4
1	0	0	0	0	0	0	1	M0:e.5
								M0:e.6
								M0:e.7
								M0:e.8

Range 1 Outputs
Range 3 Outputs
Range 5 Outputs
Range 7 Outputs
Range 9 Outputs
Range 11 Outputs

Rate Period (decimal) (page 4–12)

ATTENTION: The module will fault on power-up if you do not enter a value.

Rate Period	0	1	0	M0:e.9

1 to 255 = 10 ms to 2.55 seconds

R = Reserved, must be reset to 0

Starting and Ending Range Values (decimal) (page 4–12)

These two ranges are shown for clarity only, they do not have to be programmed because their output data is zero. Outputs are reset to 0 when ranges are not active.

Range 1 Starting Value					0	**M0:e.10**	slow feed
Range 1 Ending Value				4	9	M0:e.11	
Range 2 Starting Value				5	0	**M0:e.12**	fast feed
Range 2 Ending Value	1	0	2	4	9	M0:e.13	
Range 3 Starting Value	1	0	2	5	0	**M0:e.14**	slow feed
Range 3 Ending Value	1	9	9	9	9	M0:e.15	
Range 4 Starting Value	1	0	0	0	0	**M0:e.16**	drill
Range 4 Ending Value	1	9	9	9	9	M0:e.17	
Range 5 Starting Value	1	1	0	0	0	**M0:e.18**	stop
Range 5 Ending Value	1	9	9	9	9	M0:e.19	
Range 6 Starting Value						**M0:e.20**	
Range 6 Ending Value						M0:e.21	
Range 7 Starting Value						**M0:e.22**	
Range 7 Ending Value						M0:e.23	
Range 8 Starting Value						**M0:e.24**	
Range 8 Ending Value						M0:e25	
Range 9 Starting Value						**M0:e.26**	
Range 9 Ending Value						M0:e.27	
Range 10 Starting Value						**M0:e.28**	
Range 10 Ending Value						M0:e.29	
Range 11 Starting Value						**M0:e.30**	
Range 11 Ending Value						M0:e.31	
Range 12 Starting Value						**M0:e.32**	
Range 12 Ending Value						M0:e.33	

Reset Value/Maximum Count Value (page 4–13)

ATTENTION: The module will fault on power-up if you do not enter a value.

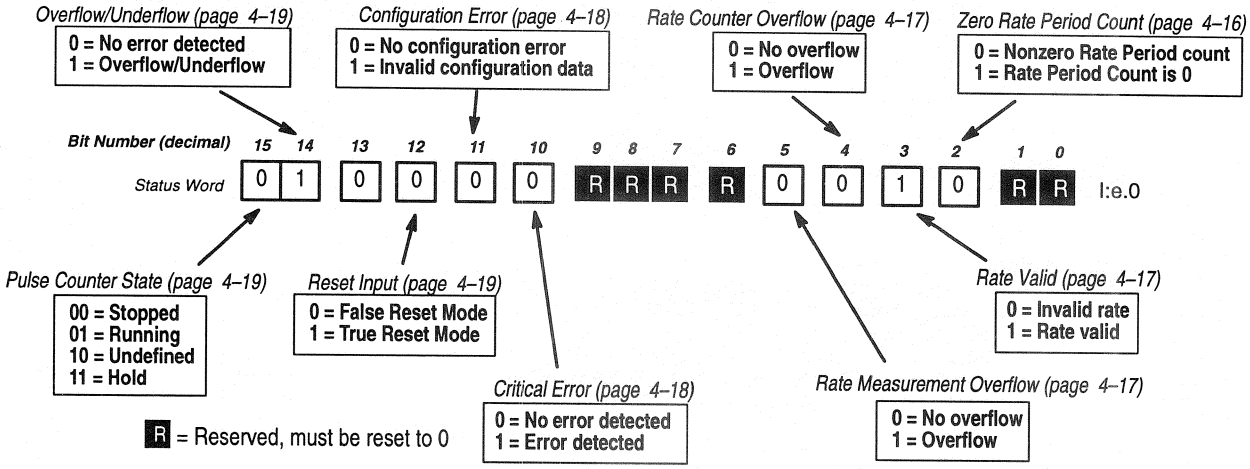
Reset Value/Maximum Count Value	0	0	0	0	0	M0:e.34

Ring counter – Maximum Count Value range is 1 to 32767 (rollover at +32767)
Linear counter – Reset Value range is –32767 to +32767.

Shown below is the Range/Rate Mode Configuration Worksheet for the Input File. A blank worksheet is supplied in appendix E.

Important: The data contained in the Input Data File varies, depending on the range that is active. The following cross section of time was taken within Ranges 2 and 4.

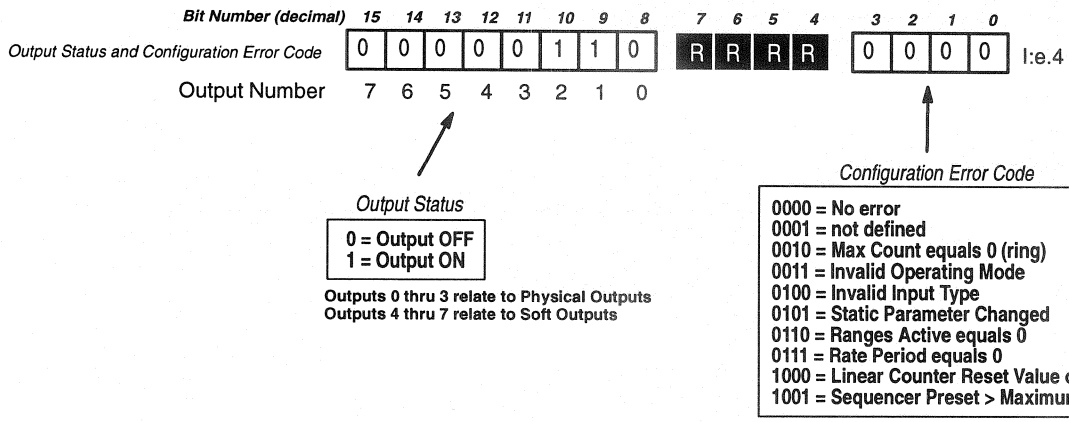
Status Word



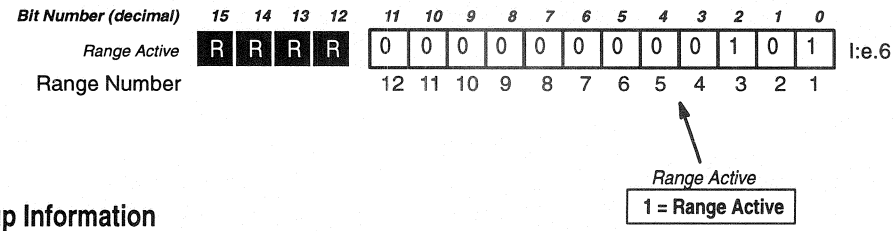
Accumulated Count, Rate Period Count, and Rate Measurement (decimal)

Accumulated Count	1	0	1	7	5	I:e.1
Rate Period Count			2	7	5	I:e.2
Rate Measurement (Hz)		2	7	5	0	I:e.3

Output Status and Configuration Error Code



Range Active

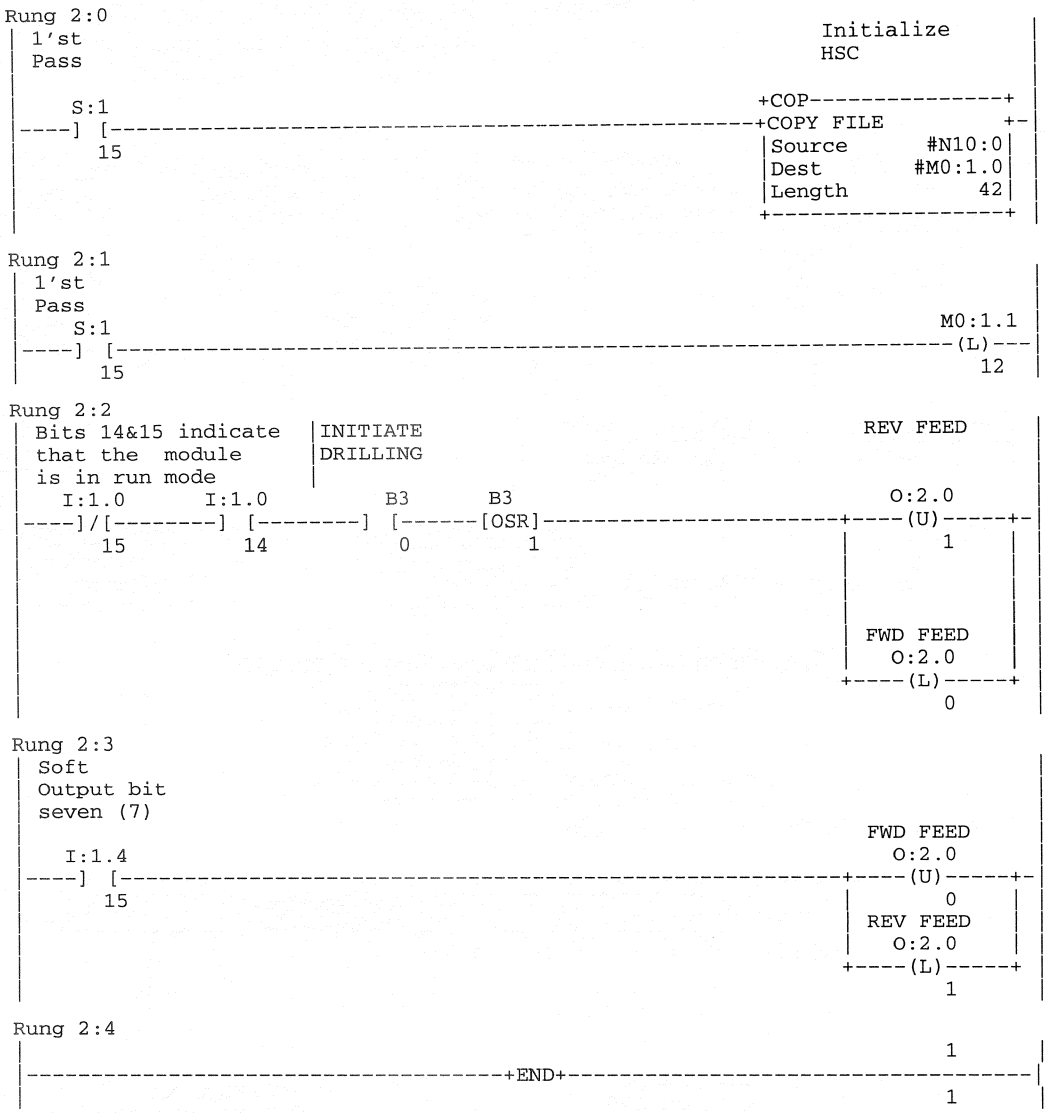


Module Setup Information

Module ID Code = 12705 (8 Input and 1 Output word) 42 M0 File words
File size – 42 word integer file, 42 word M0 File

User Program

Shown below is the user program for the drilling example.



Configuration Data Tables

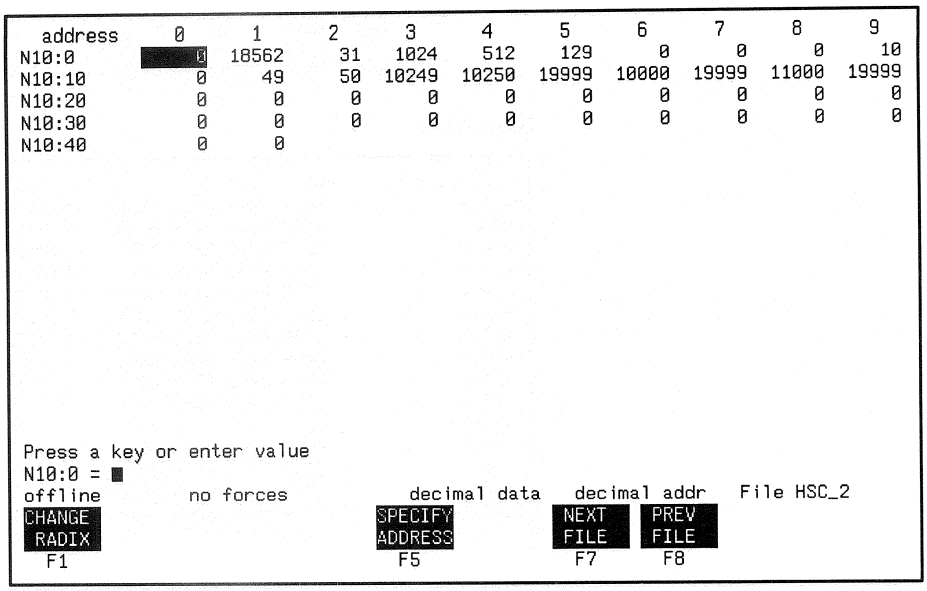
Shown below is the configuration information for the Drilling example in Binary, Decimal, and Hex radixes.

Binary Radix

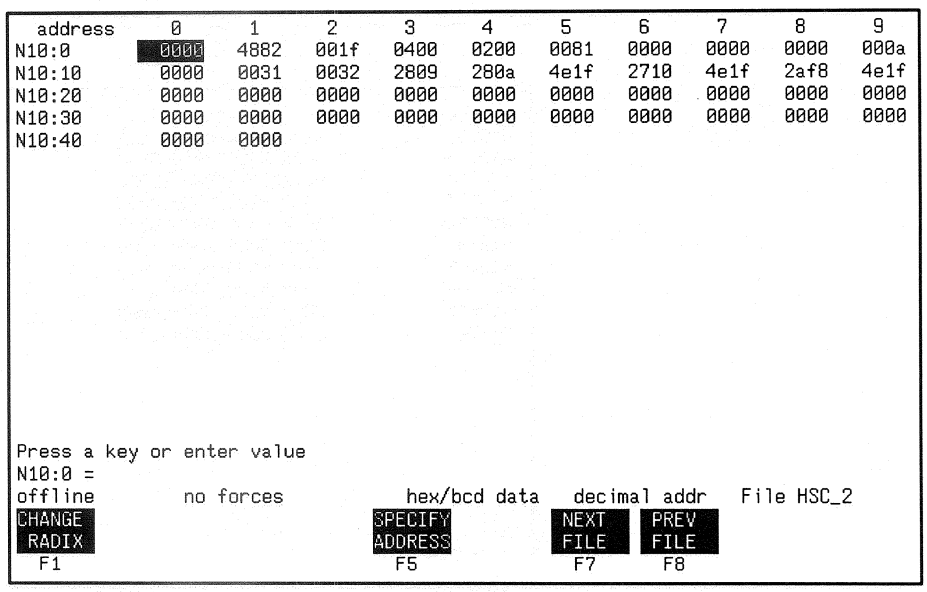
```
  address       15      data       0      address       15      data       0
N10:0            0000 0000 0000 0000    N10:16           0010 0111 0001 0000
N10:1            0100 1000 1000 0010    N10:17           0100 1110 0001 1111
N10:2            0000 0000 0001 1111    N10:18           0010 1010 1111 1000
N10:3            0000 0100 0000 0000    N10:19           0100 1110 0001 1111
N10:4            0000 0010 0000 0000    N10:20           0000 0000 0000 0000
N10:5            0000 0000 1000 0001    N10:21           0000 0000 0000 0000
N10:6            0000 0000 0000 0000    N10:22           0000 0000 0000 0000
N10:7            0000 0000 0000 0000    N10:23           0000 0000 0000 0000
N10:8            0000 0000 0000 0000    N10:24           0000 0000 0000 0000
N10:9            0000 0000 0000 1010    N10:25           0000 0000 0000 0000
N10:10           0000 0000 0000 0000    N10:26           0000 0000 0000 0000
N10:11           0000 0000 0011 0001    N10:27           0000 0000 0000 0000
N10:12           0000 0000 0011 0010    N10:28           0000 0000 0000 0000
N10:13           0010 1000 0000 1001    N10:29           0000 0000 0000 0000
N10:14           0010 1000 0000 1010    N10:30           0000 0000 0000 0000
N10:15           0100 1110 0001 1111    N10:31           0000 0000 0000 0000


Press a key or enter value
N10:0/0 =
offline        no forces          binary data    decimal addr   File HSC_2
CHANGE          SPECIFY          NEXT    PREV
 RADIX          ADDRESS          FILE    FILE
  F1              F5              F7      F8
```

```
  address       15      data       0      address       15      data       0
N10:32           0000 0000 0000 0000
N10:33           0000 0000 0000 0000
N10:34           0000 0000 0000 0000
N10:35           0000 0000 0000 0000
N10:36           0000 0000 0000 0000
N10:37           0000 0000 0000 0000
N10:38           0000 0000 0000 0000
N10:39           0000 0000 0000 0000
N10:40           0000 0000 0000 0000
N10:41           0000 0000 0000 0000




Press a key or enter value
N10:32/0 =
offline        no forces          binary data    decimal addr   File HSC_2
CHANGE          SPECIFY          NEXT    PREV
 RADIX          ADDRESS          FILE    FILE
  F1              F5              F7      F8
```

Decimal Radix



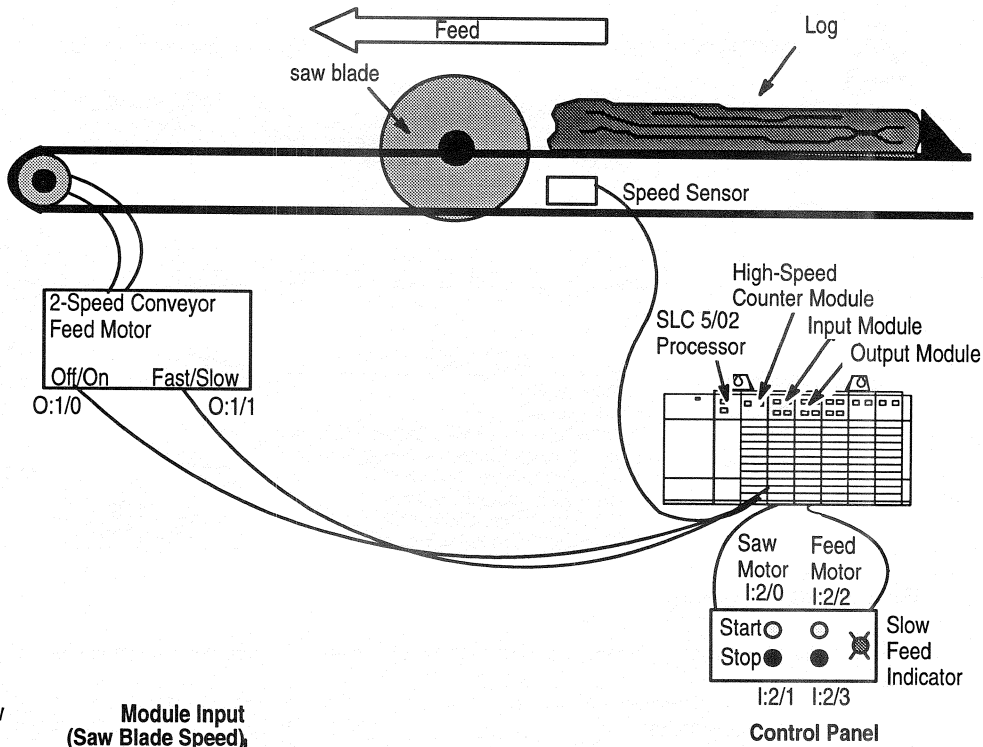
Hexadecimal Radix

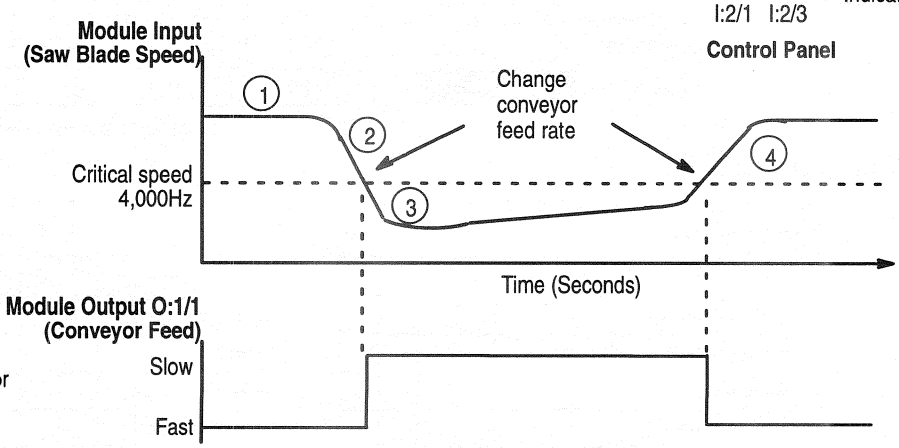


Rate Mode – Log Ripper Example

In the following rate example, a variable speed conveyor is being used to feed logs into a saw blade. An encoder is connected to the motor shaft. As the shaft turns, the encoder generates pulses and sends them to the module. The module uses the pulses to calculate the rate of the sawblade in Hz.

The conveyor has two speeds, fast and slow. Logs are fed into the saw blade in the fast speed. When the saw blade encounters an irregularity in the log (for example, a pocket of pitch or a knot) that slows the saw blade. The module detects the saw blade's reduction in speed and reduces the conveyor feed rate. Once the saw blade clears the irregularity and returns to its normal cutting speed, the module increases the conveyor feed rate.





① The conveyor feeds a log into the saw blade at a fast rate.

② The saw blade encounters an irregularity that causes the saw blade to slow down. The Slow Feed lamp illuminates.

③ The module detects the saw blades reduced speed and reduces the conveyor feed rate.

④ The saw blade clears the irregularity and returns to its normal cutting speed. The module increases the conveyor feed rate.

This simple example uses two conveyor speeds. More steps could be added to slowly ramp the conveyor speed.

Configuration Worksheets

Shown below is the Range/Rate Mode Configuration Worksheet for M0 Files. A blank worksheet is supplied in appendix E.

Direct Outputs (page 4–15)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Number								
Direct Outputs	R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	O:e.0

1 = output ON if under processor control

Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

Output Source Select (page 4–5)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Source Select	R	R	R	R	R	R	R	R

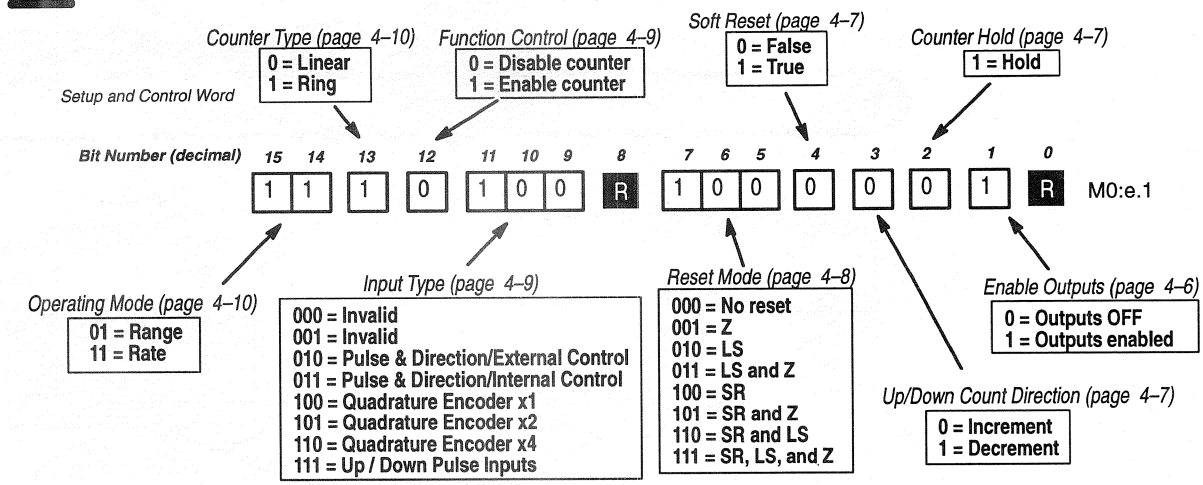
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	1	M0:e.0

1 = processor 0 = module

Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

Setup and Control Word (page 4–6)

ATTENTION: The module will fault on power-up if you do not enter a value.



Valid Ranges (page 4–11)

ATTENTION: The module will fault on power-up if you do not enter a value.

Bit Number (decimal)	15	14	13	12
Range Number				
Valid Range	R	R	R	R

11	10	9	8	7	6	5	4	3	2	1	0	
12	11	10	9	8	7	6	5	4	3	2	1	
0	0	0	0	0	0	0	0	0	0	1	1	M0:e.2

1 = range is valid. At least one range must be valid.

Range Outputs (page 4–11)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Number	7	6	5	4	3	2	1	0
Range 2 Outputs	0	0	0	0	0	0	1	0
Range 4 Outputs								
Range 6 Outputs								
Range 8 Outputs								
Range 10 Outputs								
Range 12 Outputs								

7	6	5	4	3	2	1	0	
7	6	5	4	3	2	1	0	
Range 1 Outputs	1	0	0	0	0	0	0	0	M0:e.3
Range 3 Outputs									M0:e.4
Range 5 Outputs									M0:e.5
Range 7 Outputs									M0:e.6
Range 9 Outputs									M0:e.7
Range 11 Outputs									M0:e.8

Rate Period (decimal) (page 4–12)

ATTENTION: The module will fault on power-up if you do not enter a value.

Rate Period	0	3	0	M0:e.9

1 to 255 = 10 ms to 2.55 seconds

R = Reserved, must be reset to 0

Starting and Ending Range Values (decimal) (page 4–12)

Range 1 Starting Value		4	0	0	0	**M0:e.10**	fast
Range 1 Ending Value		9	9	9	9	M0:e.11	
Range 2 Starting Value					0	**M0:e.12**	slow
Range 2 Ending Value		3	9	9	9	M0:e.13	
Range 3 Starting Value						**M0:e.14**	
Range 3 Ending Value						M0:e.15	
Range 4 Starting Value						**M0:e.16**	
Range 4 Ending Value						M0:e.17	
Range 5 Starting Value						**M0:e.18**	
Range 5 Ending Value						M0:e.19	
Range 6 Starting Value						**M0:e.20**	
Range 6 Ending Value						M0:e.21	
Range 7 Starting Value						**M0:e.22**	
Range 7 Ending Value						M0:e.23	
Range 8 Starting Value						**M0:e.24**	
Range 8 Ending Value						M0:e25	
Range 9 Starting Value						**M0:e.26**	
Range 9 Ending Value						M0:e.27	
Range 10 Starting Value						**M0:e.28**	
Range 10 Ending Value						M0:e.29	
Range 11 Starting Value						**M0:e.30**	
Range 11 Ending Value						M0:e.31	
Range 12 Starting Value						**M0:e.32**	
Range 12 Ending Value						M0:e.33	

Reset Value/Maximum Count Value (page 4–13)

ATTENTION: The module will fault on power-up if you do not enter a value.

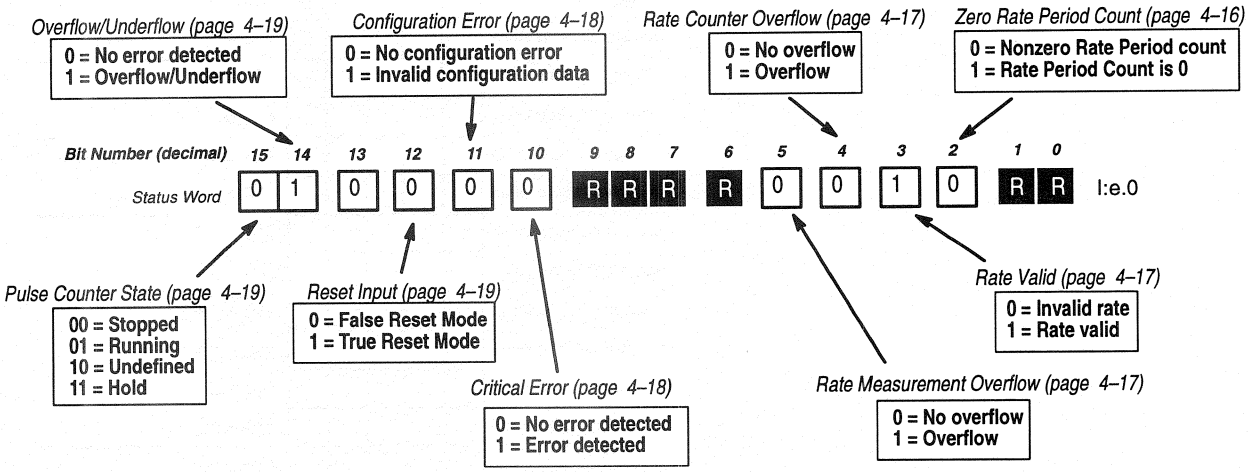
Reset Value/Maximum Count Value	3	2	7	6	7	M0:e.34

Ring counter – Maximum Count Value range is 1 to 32767 (rollover at +32767)
Linear counter – Reset Value range is –32767 to +32767.

Shown below is the Range/Rate Mode Configuration Worksheet for the Input File. A blank worksheet is supplied in appendix E.

Important: The data contained in the Input Data File varies, depending on the range that is active. The following cross section of time was taken while the conveyor was moving in the fast speed (6500 Hz).

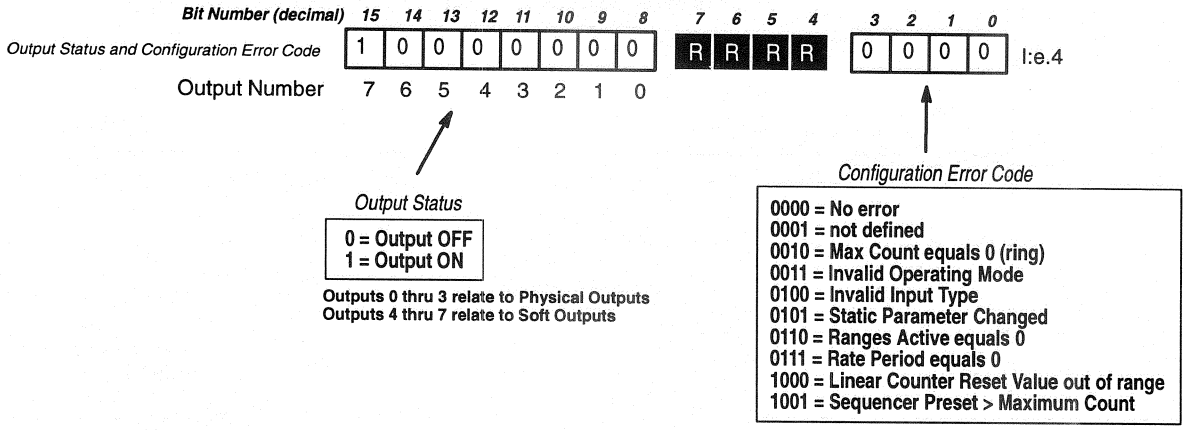
Status Word



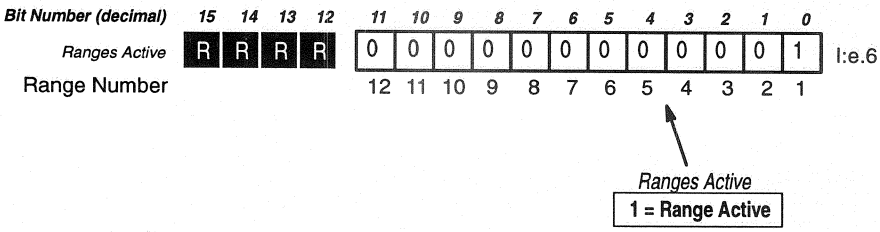
Accumulated Count, Rate Period Count, and Rate Measurement (decimal)

Accumulated Count		9	8	7	6	I:e.1
Rate Period Count		1	9	5	0	I:e.2
Rate Measurement (Hz)		6	5	0	0	I:e.3

Output Status and Configuration Error Code



Ranges Active

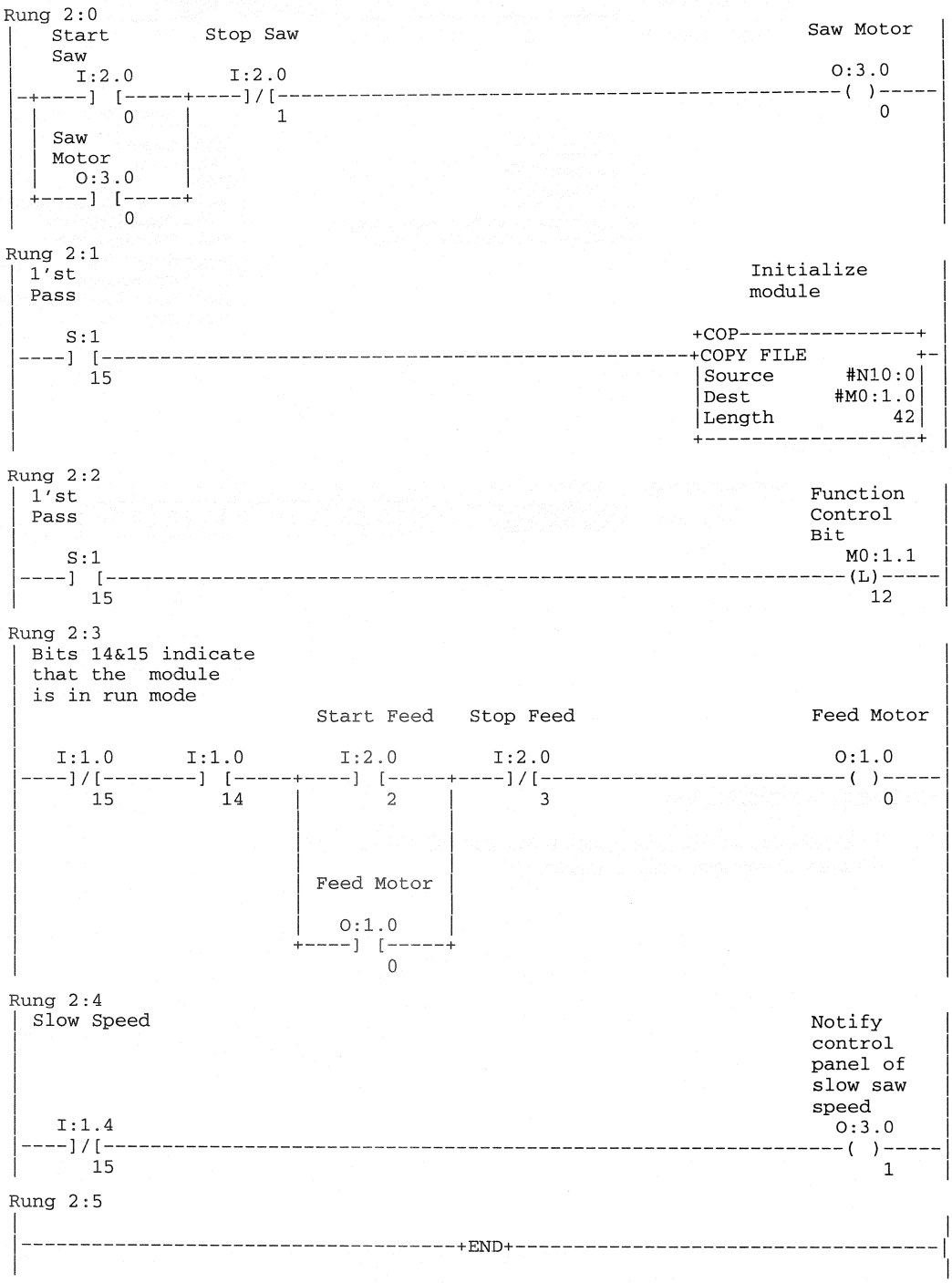


Module Setup Information

Module ID Code = 12705 (8 Input and 1 Output word) 42 M0 File words
File size – 42 word integer file, 42 word M0 File

User Program

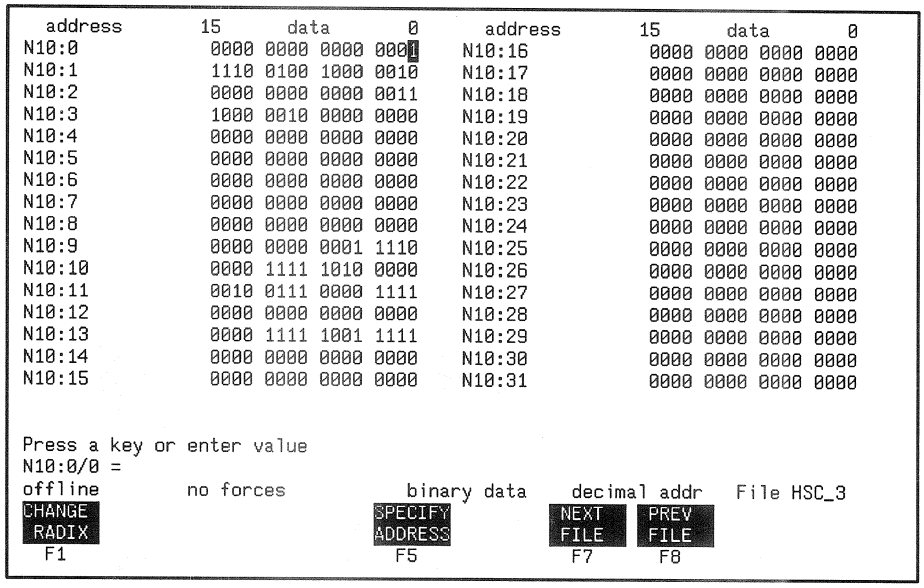
Shown below is the user program for the Log Ripper example.

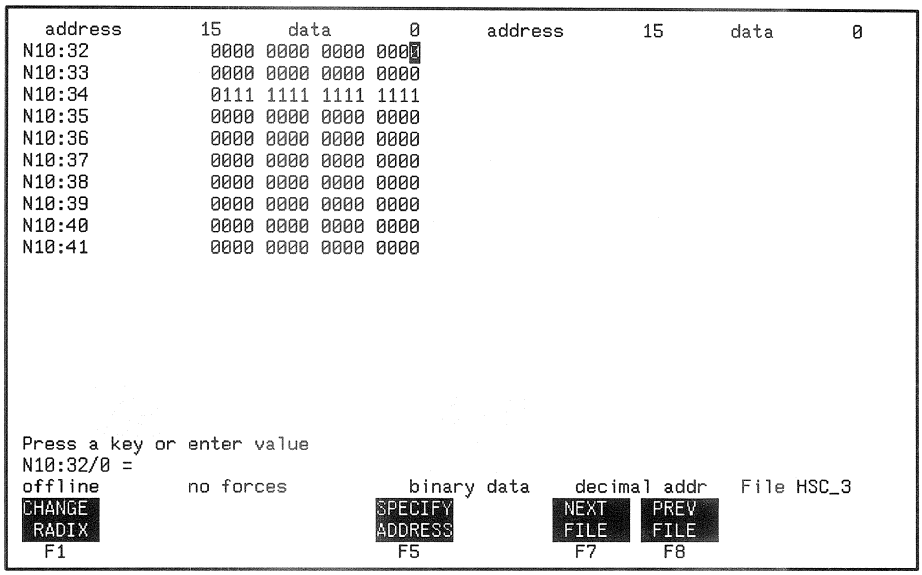


Configuration Data Tables

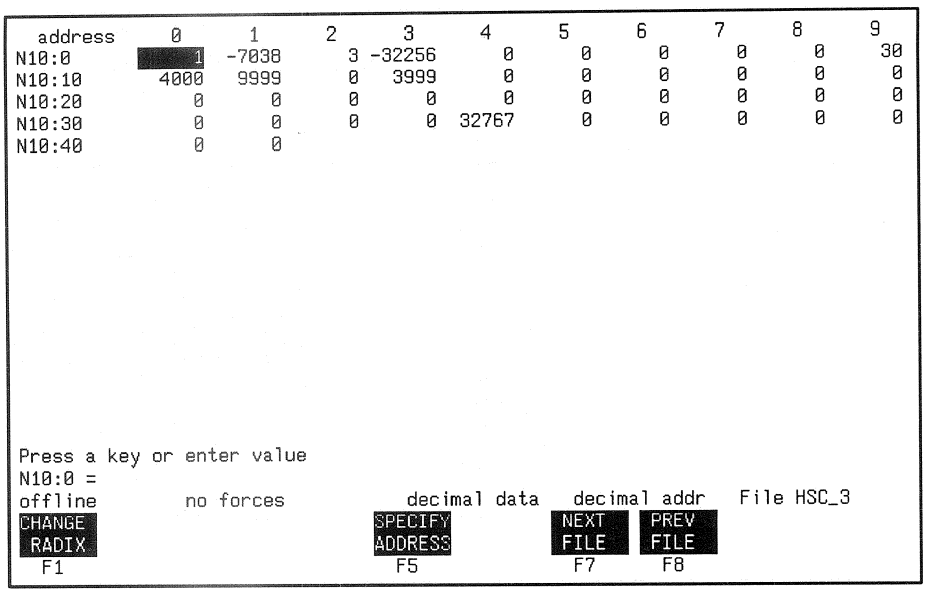
Shown below is the configuration information for the Log Ripper example in Binary, Decimal, and Hex radixes.

Binary Radix

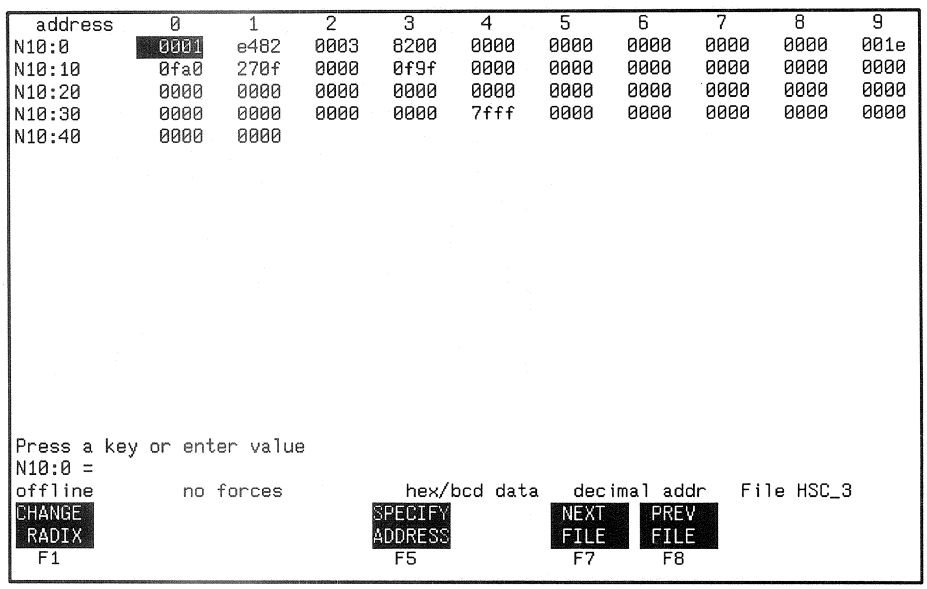




Decimal Radix



Hexadecimal Radix



Sequencer Mode – Cut to Length Example

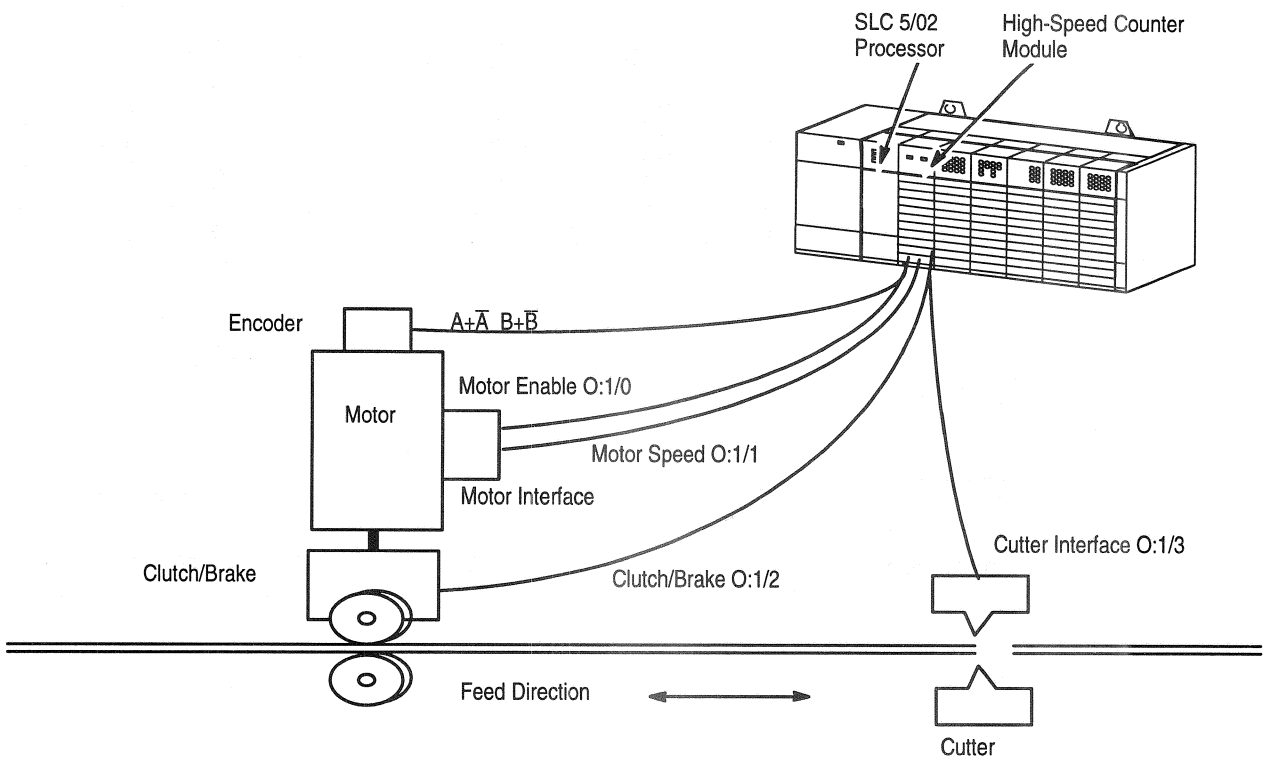
In this example, flat steel is fed into a cutter. Using the Sequencer Mode, it is cut to a specific length. The application consists of a motor, motor interface, encoder, clutch/brake, and cutter.

A quadrature encoder is connected directly to the motor shaft. It sends pulses to the module. The module controls the motor interface.

The motor interface controls the motor speed, the user program enables the motor. When O:1/0 is energized, the motor is enabled. The motor operates in two speeds, low and high. When the output (O:1/1) is energized, the motor is running in high-speed mode.

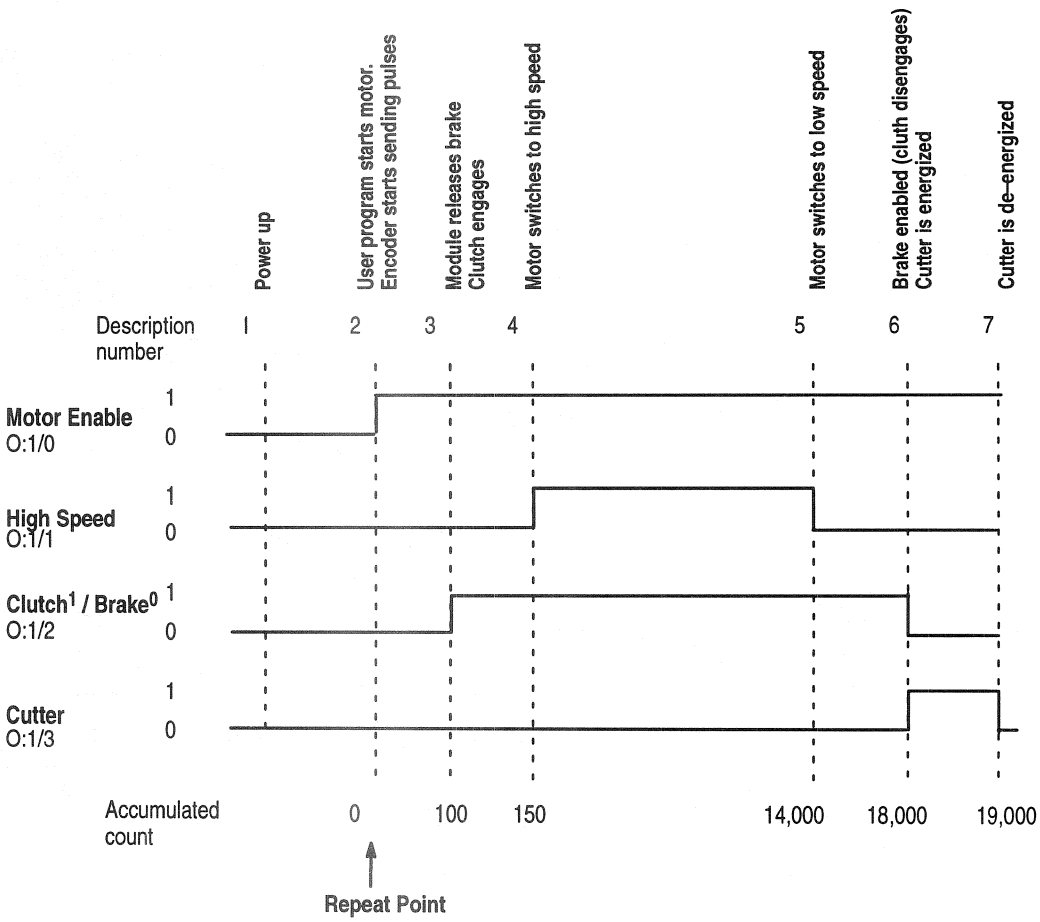
The clutch/brake has two states. The clutch is engaged when O:1/2 is energized. Engaging the clutch feeds the steel into the cutter. The brake is engaged when O:1/2 is de-energized.

The cutter is controlled by the module and is self retracting when the power is off. It also has its own end of travel mechanism.



The following is a brief description of the application.

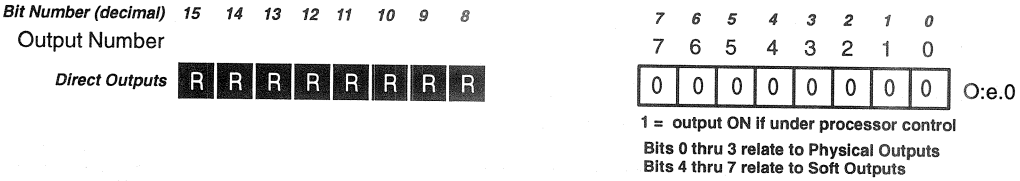
1. The Initial Outputs (M0:e.3/8–15) are reset to 0. Therefore, the brake is enabled (the clutch is disengaged) and the cutter is retracted.
2. The user program starts the motor. The encoder begins to send pulses to the module.
3. After 100 counts, the module releases the brake (O:1/2), which engages the clutch.
4. At count 150, the high-speed motor output (O:1/1) is energized.
5. At count 14000, the high-speed motor output (O:1/1) is de-energized.
6. At count 18000, the brake is enabled (which disables the clutch) and the cutter is energized.
7. At count 19000, the cutter is de-energized and the sequencer rolls over. The process repeats, as indicated below by the repeat point.



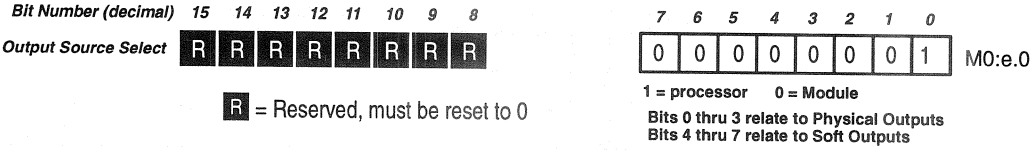
Configuration Worksheets

Shown below is the Sequencer Mode Configuration Worksheet for the Output and M0 File. A blank worksheet is supplied in appendix F.

Direct Outputs (page 4–32)

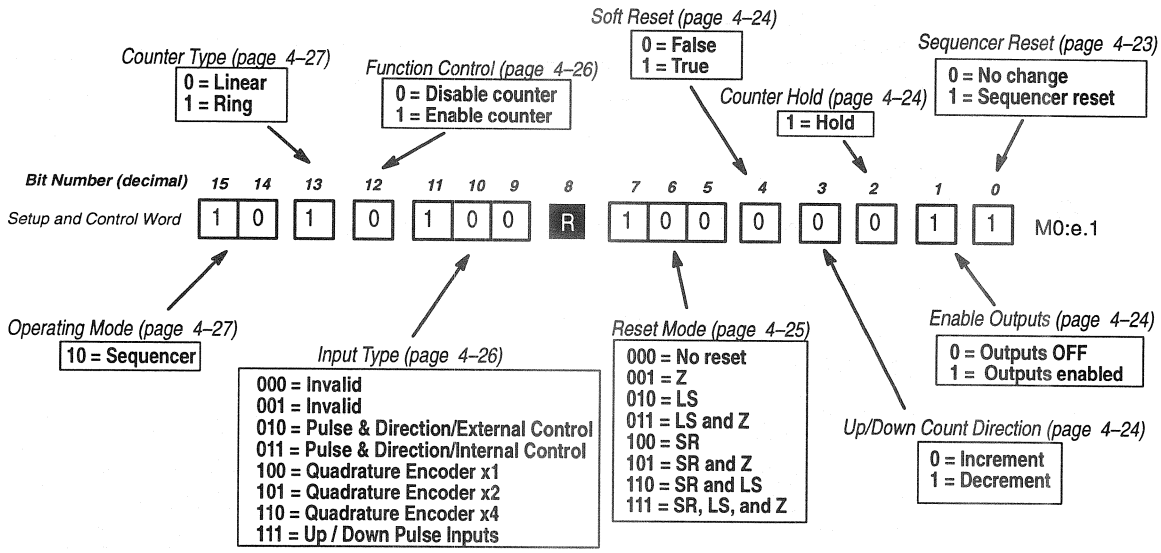


Output Source Select (page 4–22)



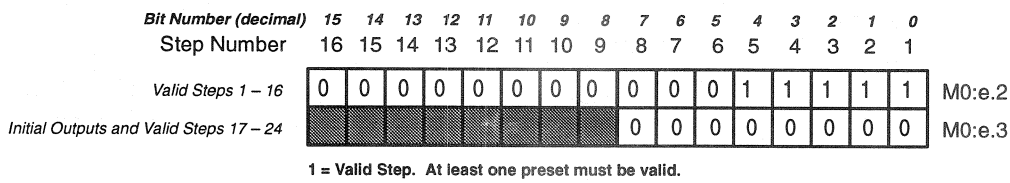
Setup and Control Word (page 4–23)

ATTENTION: The module will fault on power-up if you do not enter a value.

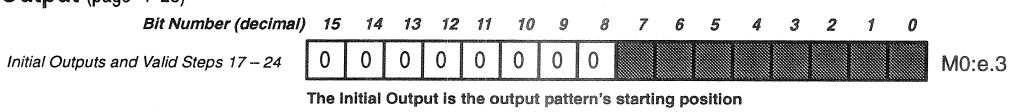


Valid Steps (page 4–28)

ATTENTION: The module will fault on power-up if you do not enter a value.



Initial Output (page 4–28)



Shown below is a Sequencer Mode Configuration Worksheet for Step Output information. Based on your application, you enter the Step Outputs, Step Preset Values, and Reset Value/Maximum Count Value into the appropriate places on the worksheet. When you begin programming, you can transcribe the information contained in the worksheet to your data files. A blank worksheet is supplied in appendix F.

Step Outputs (page 4–29)

Bit Number (decimal)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Output Number	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Step 1 Outputs									0	0	0	0	0	1	0	0	**M0:e.4**
Step 2 Outputs	1	0	0	0	0	1	1	0									
Step 3 Outputs									0	0	0	0	0	1	0	0	M0:e.5
Step 4 Outputs	0	0	0	0	1	0	0	0									
Step 5 Outputs									0	0	0	0	0	0	0	0	**M0:e.6**
Step 6 Outputs																	
Step 7 Outputs																	M0:e.7
Step 8 Outputs																	
Step 9 Outputs																	**M0:e.8**
Step 10 Outputs																	
Step 11 Outputs																	M0:e.9
Step 12 Outputs																	
Step 13 Outputs																	**M0:e.10**
Step 14 Outputs																	
Step 15 Outputs																	M0:e.11
Step 16 Outputs																	
Step 17 Outputs																	**M0:e.12**
Step 18 Outputs																	
Step 19 Outputs																	M0:e.13
Step 20 Outputs																	
Step 21 Outputs																	**M0:e.14**
Step 22 Outputs																	
Step 23 Outputs																	M0:e.15
Step 24 Outputs																	

Rate Period (decimal) (page 4–30)

ATTENTION: The module will fault on power-up if you do not enter a value.

Rate Period	0	1	0	M0:e.16

1 to 255 = 10 ms to 2.55 seconds

Step Preset Values (decimal) (page 4–30)

Step 1 Preset				9	9	**M0:e.17**	*Step 13 Preset*						M0:e.29
Step 2 Preset			1	4	9	M0:e.18	*Step 14 Preset*						**M0:e.30**
Step 3 Preset	1	3	9	9	9	**M0:e.19**	*Step 15 Preset*						M0:e.31
Step 4 Preset	1	7	9	9	9	M0:e.20	*Step 16 Preset*						**M0:e.32**
Step 5 Preset	1	8	9	9	9	**M0:e.21**	*Step 17 Preset*						M0:e.33
Step 6 Preset						M0:e.22	*Step 18 Preset*						**M0:e.34**
Step 7 Preset						**M0:e.23**	*Step 19 Preset*						M0:e.35
Step 8 Preset						M0:e.24	*Step 20 Preset*						**M0:e.36**
Step 9 Preset						**M0:e.25**	*Step 21 Preset*						M0:e.37
Step 10 Preset						M0:e.26	*Step 22 Preset*						**M0:e.38**
Step 11 Preset						**M0:e.27**	*Step 23 Preset*						M0:e.39
Step 12 Preset						M0:e.28	*Step 24 Preset*						**M0:e.40**

Reset Value/Maximum Count Value (page 4–31)

ATTENTION: The module will fault on power-up if you do not enter a value.

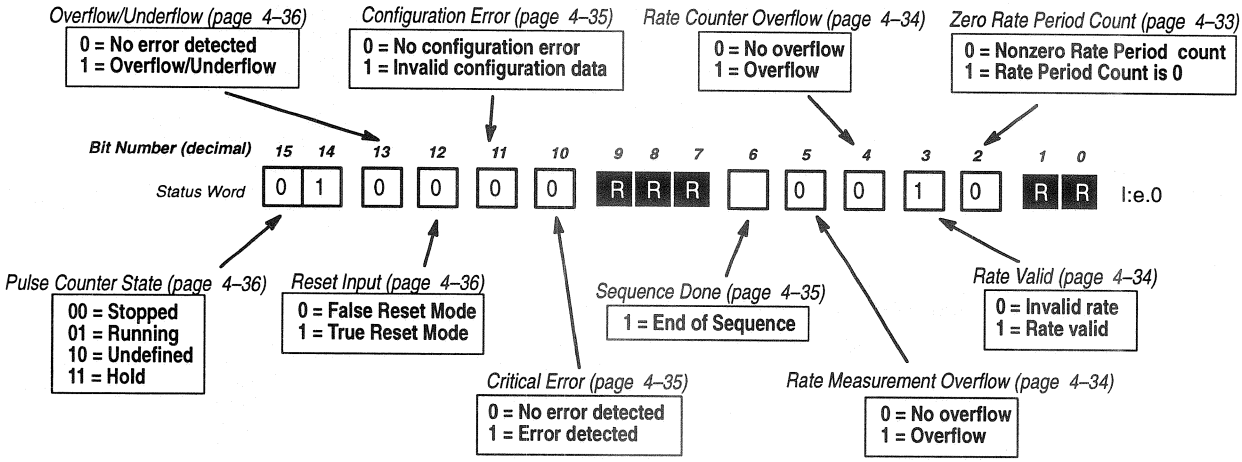
Reset Value/Maximum Count Value | 1 | 8 | 9 | 9 | 9 | M0:e.41

Ring counter – Maximum Count Value range is 1 to 32767 (rollover at +32767)
Linear counter – Reset Value range is –32767 to +32767.

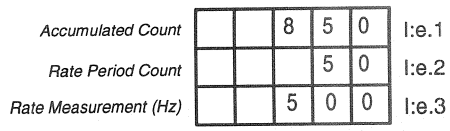
Shown below is the Sequencer Mode Configuration Worksheet for the Input Data File. A blank worksheet is supplied in appendix F.

Important: The data contained in the Input Data File varies, depending on the step number. The following cross section of time was taken 700 counts after the Step 2 Preset was reached.

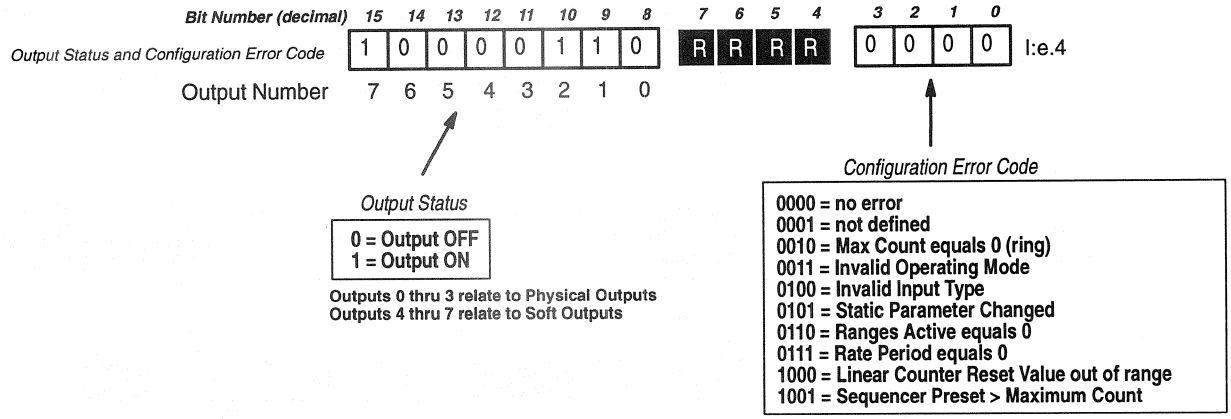
Status Word



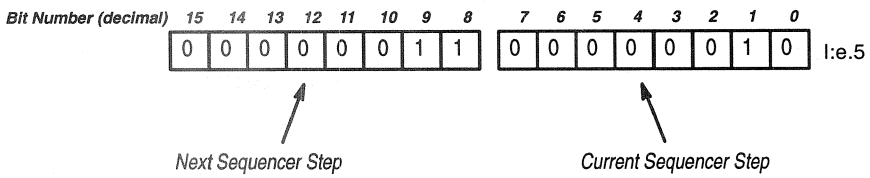
Accumulated Count, Rate Period Count, and Rate Measurement (decimal)



Output Status and Configuration Error Code



Next Sequencer Step and Current Sequencer Step



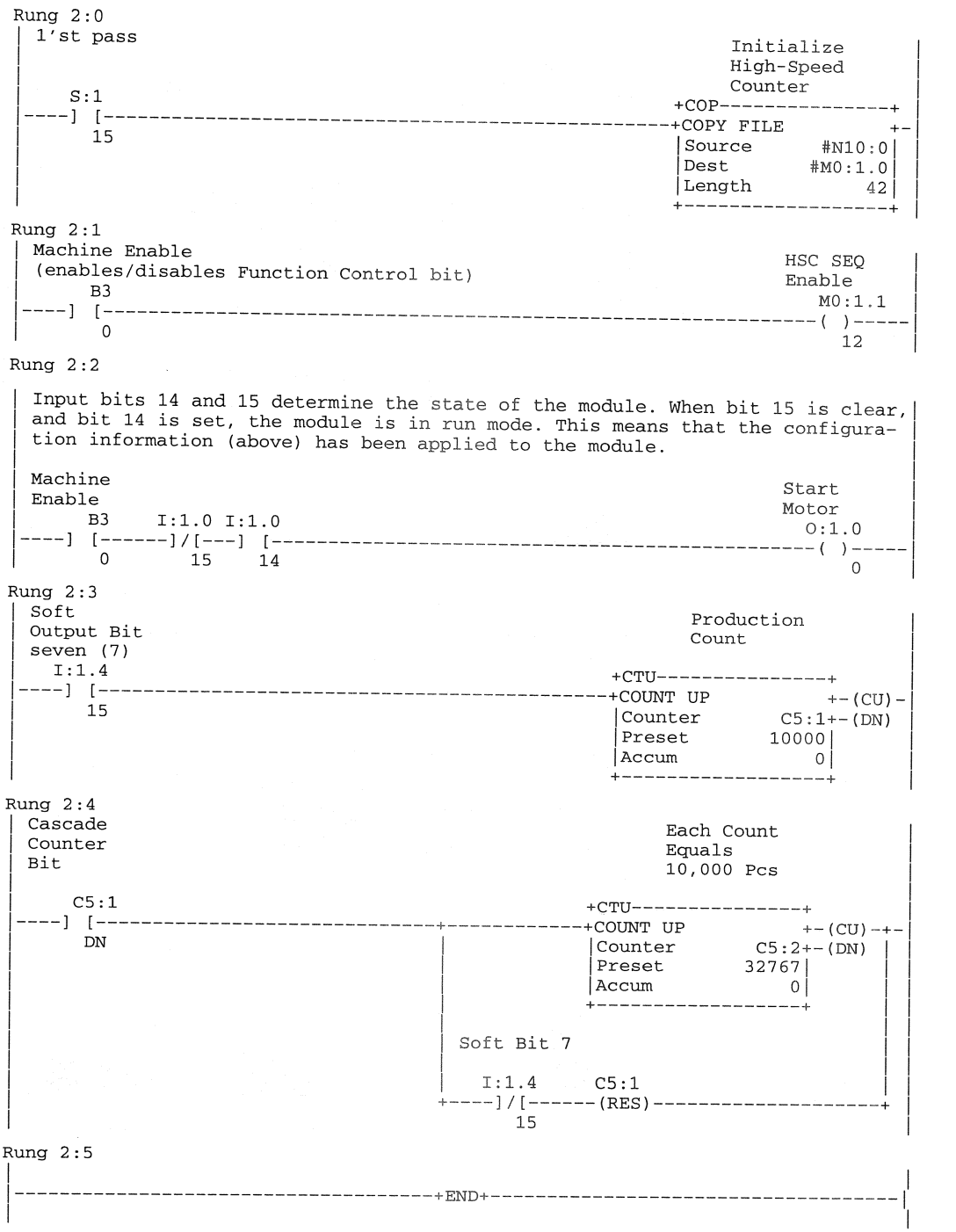
Next Sequencer Step Preset (decimal)

Module Setup Information

Module ID Code = 12705 (8 Input and 1 Output word)
File Size – 42 word integer file, and 42 word M0 File

User Program

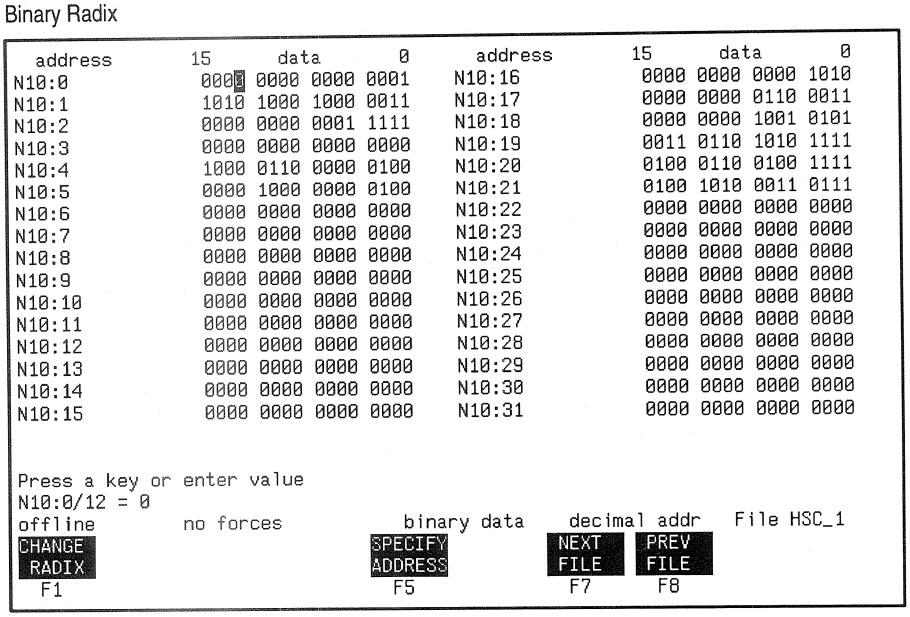
Shown below is the user program for the Cut to Length example.

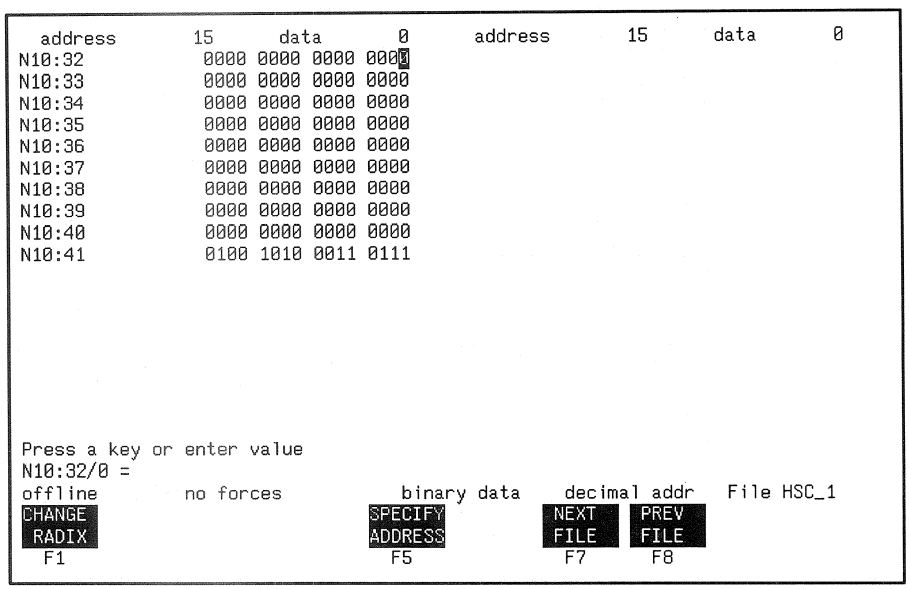


Configuration Data Tables

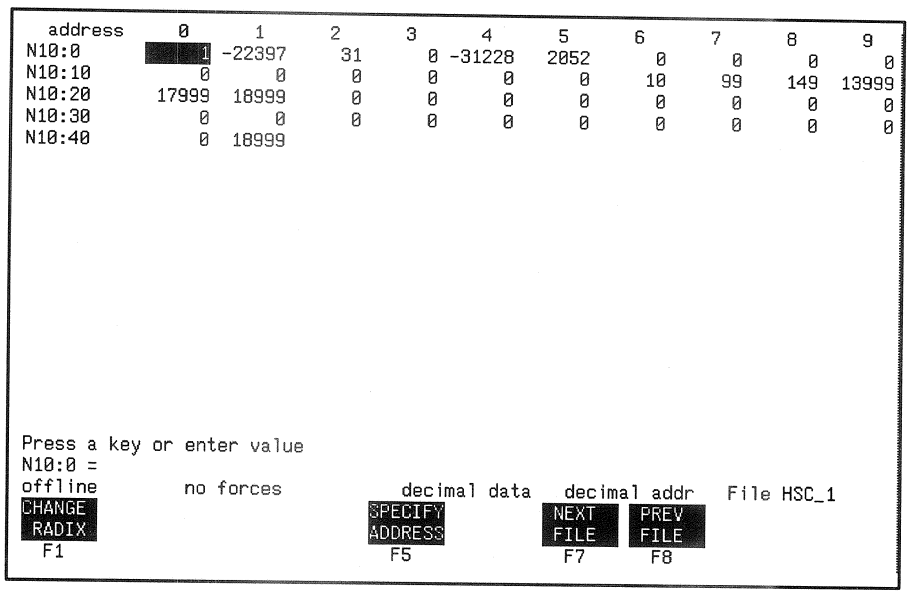
Shown below is the configuration information for the Cut to Length example in Binary, Decimal, and Hex radixes.

Binary Radix

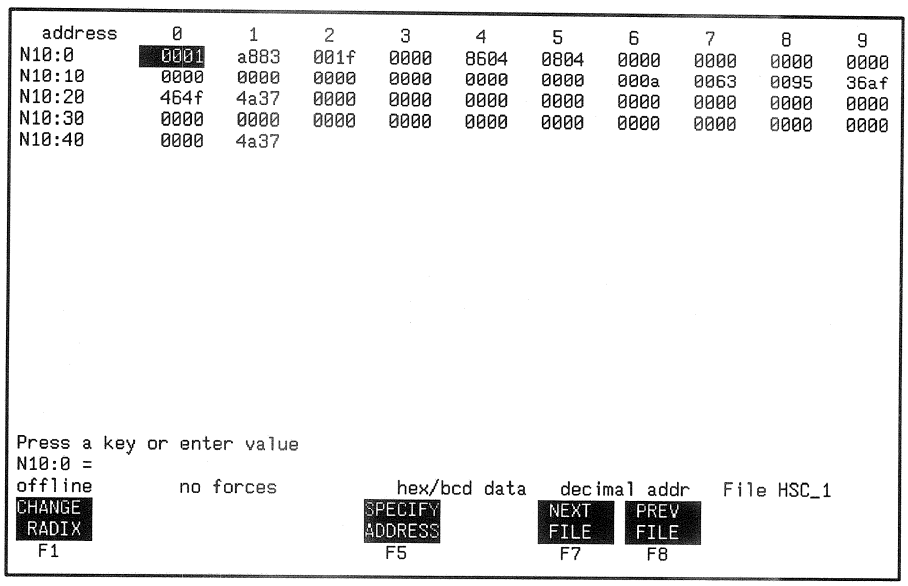




Decimal Radix



Hexadecimal Radix



Specifications

General

Operating Temperature	0°C to +60°C (+32°F to +140°F)
Storage Temperature	–40°C to +85°C (–40°F to +185°F)
Humidity	5 to 95% without condensation
Backplane Current Consumption (power supply loading)	320 mA at +5V 0 mA at +24V
Maximum Cable Length①	305 m (1000 ft)
Agency Certification (when product or packaging is marked)	• CSA certified • CSA Class I, Division 2 Groups A, B, C, D certified • UL listed • CE marked for all applicable directives

① Belden 9503 or equivalent

Inputs A, B, and Z

	Differential (Switch 1 on)	Single Ended (Switch 1 off)
Input Voltage	±5V dc	0 to 5V dc①
On-State Voltage	2.8 to 4.5V dc	3.1 to 5.5V dc
OFF-State Voltage	–5.5 to 0.8V dc	0 to 0.8V dc
Max Off-State Leakage Current	100 µA	600 µA
Input Current (mA)	2.5 mA at 2.8V dc 7.5 mA at 4.5V dc	2.5 mA at 3.1V dc 7.5 mA at 5.5V dc
Nominal Input Impedance	700Ω	825Ω
Min. Pulse Width	10 µs	
Min. Phase Separation②	4.5 µs	
Max. Input Frequency **Sequencer and Range Rate**	 50k Hz 32.767k Hz	
Isolation (from backplane)	1500 volts	

① 12 and 24 volts must be used with a pullup resistor

② Channel A to channel B

Limit Switch Input

	5V dc	12V dc	24V dc
On-State Voltage	3.8 to 5.4V dc	9.4 to 16.5V dc	16.5 to 30V dc
Off-State Voltage	0 to 1.2V dc	0 to 2.4V dc	0 to 3.9V dc
Input Current minimum nominal maximum	 4.6 mA 6.8 mA 9.2 mA		
Max. Off-State Leakage Current	1 mA (all ranges)		
Isolation (from backplane)	1500 volts		

Outputs (Open Collector, Sinking)

	4.5 to 10V dc (Switch 2 on)	10 to 30V dc (Switch 2 off)
Max. On-State Output Current	16 mA at 4.5V dc 40 mA at 10V dc	40 mA at 10V dc 125 mA at 30V dc
Max. On-State Voltage Drop	0.4V dc	1.0V dc
Max. Off-State Leakage Current	100 µA	
Isolation (from backplane)	1500 volts	

Timing Information

Operation	Description	Timing[1]
Throughput	The delay time between the module receiving a pulse and the updating of its physical outputs.	Sequencer: 1.8 ms Range: 3.9 ms Rate: 70.0 ms + Rate Period
Minimum wait time between range boundaries	Minimum amount of time (between range or step boundaries) required to ensure a range or sequencer step is not missed.	Sequencer: 2.5 ms Range: 3.0 ms Rate: 70.0 ms + Rate Period
Input file update time	The time required for the module to make a change of input status (I:e.0 to I:e.7) available to the user program.	Sequencer: 45 ms Range: 60 ms Rate: 35 ms
Physical output response time (under SLC control)	The time required for the module's Direct Outputs Field to respond to control commands from the user program.	Sequencer: 45 ms Range: 60 ms Rate: 35 ms
Z input reset response time. Reset to zero (0)	The time required for the module to respond to an external Z input event and reset the pulse counter to 0.	4.0 µs[2]
Z input reset response time. Reset to a value other than zero (0)	The time required for the module to respond to an external Z input event and reset the pulse counter to a value other than 0.	500 µs[2]
Limit switch reset response time. Reset to zero (0)	The time required for the module to respond to an external limit switch event and reset the pulse counter to 0.	1.0 ms with 300 µs filter[2] 15.0 ms with 10 ms filter[2]
Limit switch reset response time. Reset to a value other than zero (0)	The time required for the module to respond to an external limit switch event and reset the pulse counter to a value other than 0.	1.0 ms with 300 µs filter[2] 15.5 ms with 10 ms filter[2]
Soft Reset response time (to 0 or value other than 0)	The time required for the module to respond to a soft reset event (i.e. issued from the user program) and reset the pulse counter to 0 or a value other than 0.	Sequencer: 40 ms[2] Range: 55 ms[2] Rate: 35 ms[4]
Counter Hold response time	The time required for the module to respond to a Counter Hold command issued from the user program.	Sequencer: 35 ms Range: 50 ms Rate: 35 ms[4]
Count Direction response time via user program	The time required for the module to respond to an Up/Down Count Direction change issued from the user program.	Sequencer: 40 ms Range: 55 ms Rate: 35 ms
Dynamic Parameter response time (worst case)	The amount of time (worst case) the module needs to reconfigure data after its Dynamic Parameters have been changed (i.e. time to accept Preset change).	Sequencer: 110 ms Range: 110 ms Rate: 65 ms
Module set up time (worst case)	The time (worst case) required for the module to respond to counts received *after* the false to true transition of the Function Control bit.	Sequencer: 200 ms Range: 200 ms Rate: 200 ms
Minimum time between resets via Z input	The minimum time between Z input resets to ensure a reset response.	Sequencer: 2.0 ms Range: 3.5 ms
Minimum time between resets via limit switch with 300 µs filter	The minimum time between limit switch resets required to ensure a reset response using the 300 µs filter.	Sequencer: 2.0 ms Range: 3.5 ms
Minimum time between resets via limit switch with 10 ms filter	The minimum time between limit switch resets required to ensure a reset response using the 10 ms filter.	Sequencer: 14.0 ms Range: 17.5 ms
Interrupt latency delay time[3] (other modules)	Altering the state of the slot enable bit in the processor status file could increase the interrupt service time of the module generating the interrupt an additional 17.4 ms	17.4 ms increase

[1] Excluding SLC scan time

[2] If counts occur at the modules inputs during a reset, they may be lost for the amount of time equal to the reset response time.

[3] Currently no modules are available that generate interrupts.

[4] Rate counter not affected.

M0-M1 Files, G Files, and Interrupts

The High-Speed Counter module only uses M0 files. This appendix contains important information you should be concerned with when applying M0–M1 files, G files, and Interrupts. The information is general in nature and supplements specific information contained in earlier chapters of this manual. Topics include:

- M0–M1 files
- G files
- interrupt operation
- I/O Interrupt Disable (IID) and I/O Interrupt Enable (IIE)
- Reset Pending Interrupt (RPI)
- Interrupt Subroutine (INT)

M0–M1 Files

M0 and M1 files are data files that reside in specialty I/O modules only. There is no image for these files in the processor memory. The application of these files depends on the function of the particular specialty I/O module. For some modules, the M0 file is regarded as a module output file and the M1 file is regarded as a module input file. In any case, both M0 and M1 files are considered read/write files by the SLC 5/02, SLC 5/03, and SLC 5/04 processors.

M0 and M1 files can be addressed in your ladder program and they can also be acted upon by the specialty I/O module – independent of the processor scan. It is important that you keep the following in mind in creating and applying your ladder logic:

Important: During the processor scan, M0 and M1 data can be changed *by the processor* according to ladder diagram instructions addressing the M0 and M1 files. During the same scan, the *specialty I/O module* can change M0 and M1 data, *independent* of the rung logic applied during the scan.

Configuring M0–M1 Files Using APS Software

M0 and M1 files are configured as part of the I/O configuration procedure for the processor file. After you have assigned the specialty I/O module to a slot (the procedure is the same as assigning other modules except that you must specify the ID code of the specialty I/O module), the following functions appear at the bottom of the APS screen:

READ CONFIG	ONLINE CONFIG		MODIFY RACKS	MODIFY SLOT	DELETE SLOT	UNDEL SLOT	EXIT	SPIO CONFIG
F1	F2		F4	F5	F6	F7	F8	F9

Complete the following steps to configure the M0 and M1 files:

1. Press [F9], Specialty I/O Configuration. The following functions appear:

ISR NUMBER		MODIFY G FILE		ADVNCD SETUP		G FILE SIZE
F1		F3		F5		F7

2. Press [F5], Advanced Setup. The following functions appear:

INPUT SIZE	OUTPUT SIZE	SCANNED INPUT	SCANNED OUTPUT	M0 FILE SIZE	M1 FILE SIZE
F1	F2	F3	F4	F5	F6

3. Press [F5], then enter the number of M0 file words required (the required number is listed in the user manual for the specific specialty I/O module).
4. Press [F6], then enter the number of M1 file words required (the required number is listed in the user manual for the specific specialty I/O module).

The specialty I/O module may require that you also configure the G file and specify an ISR (interrupt subroutine) number. These tasks are accomplished with function keys F1, F3, and F7 shown in step 1 above. G files are discussed later in this appendix.

Addressing M0–M1 Files

The addressing format for M0 and M1 files is below:

Mf:e.s/b

Where	**M**	=	**module**
	f	=	**file type (0 or 1)**
	e	=	**slot (1-30)**
	s	=	**word (0 to max. supplied by module)**
	b	=	**bit (0-15)**

Restrictions on Using M0-M1 Data File Addresses

M0 and M1 data file addresses can be used in all instructions except the OSR instruction and the instruction parameters noted below:

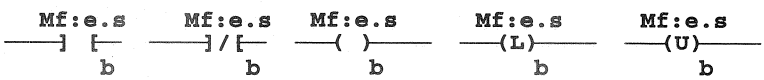
Instruction	Parameter (uses file indicator #)
BSL, BSR	File (bit array)
SQO, SQC, SQL	File (sequencer file)
LFL, LFU	LIFO (stack)
FFL, FFU	FIFO (stack)

Monitoring Bit Addresses

For SLC 5/02 processors, the M0/M1 Monitoring option is always disabled. (This processor does not allow you to monitor the actual state of each addressed M0/M1 address.) For SLC 5/03 and SLC 5/04 processors, you can choose to disable or enable the monitoring option.

M0/M1 Monitoring Option Disabled

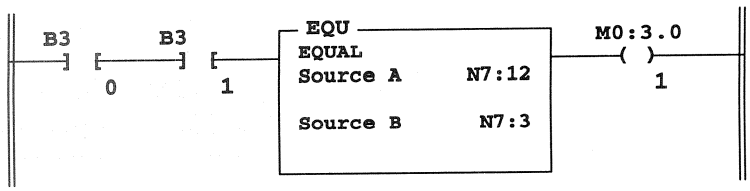
When you monitor a ladder program in the Run or Test mode with the M0/M1 Monitoring option disabled, the following bit instructions, addressed to an M0 or M1 file, are indicated as false regardless of their actual true/false logical state.



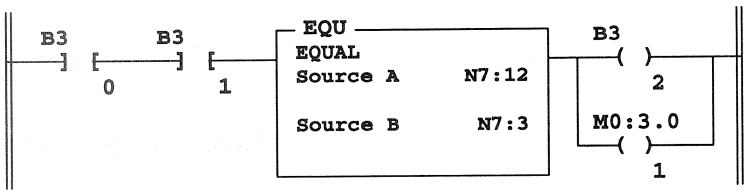
f = file (0 or 1)

When you are monitoring the ladder program in the Run or Test mode, the APS or HHT display does not show these instructions as being true when the processor evaluates them as true.

If you need to show the state of the M0 or M1 addressed bit, you can transfer the state to an internal processor bit. This is illustrated below, where an internal processor bit is used to indicate the true/false state of a rung.



This rung will not show its true rung state because the EQU instruction is always shown as true and the M0 instruction is always shown as false.



OTE instruction B3/2 has been added to the rung. This instruction shows the true or false state of the rung.

M0/M1 Monitoring Option Enabled

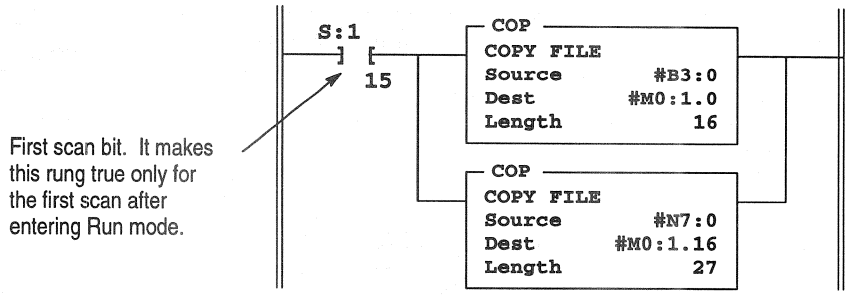
Important: This option is not supported by the SLC 5/02 processor.

The SLC 5/03 and SLC 5/04 processors allow you to monitor the actual state of each addressed M0/M1 address (or data table). The highlighting appears normal when compared to the other processor data files. The processor's performance will be degraded to the degree of M0/M1 referenced screen data. For example, if your screen has only one M0/M1 element, degradation will be minimal. If your screen has 69 M0/M1 elements, degradation will be significant.

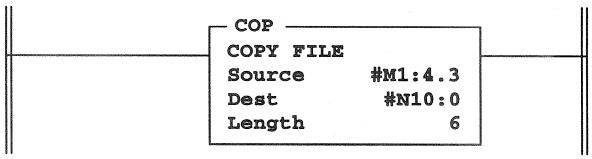
Transferring Data Between Processor Files and M0 or M1 Files

As pointed out earlier, the processor does not contain an image of the M0 or M1 file. As a result, you must edit and monitor M0 and M1 file data via instructions in your ladder program. For example, you can copy a block of data from a processor data file to an M0 or M1 data file or vice versa using the COP instruction in your ladder program.

The COP instructions below copy data from a processor bit file and integer file to an M0 file. Suppose the data is configuration information affecting the operation of the specialty I/O module.



The COP instruction below copies data from an M1 data file to an integer file. This technique is used to monitor the contents of an M0 or M1 data file indirectly, in a processor data file.



Access Time

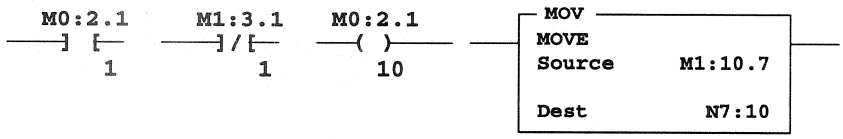
During the program scan, the processor must access the specialty I/O card to read/write M0 or M1 data. This access time must be added to the execution time of each instruction referencing M0 or M1 data. For the SLC 5/03 and SLC 5/04 processors, the instruction types vary in their execution times.

The following table shows the expected maximum access times per instruction or word of data for the SLC 5/02, SLC 5/03, and SLC 5/04 processors.

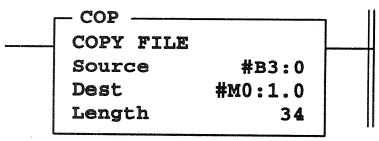
Processor	Instruction Type	Access Time per Bit Instruction or Word of Data	Access Time per Multi-Word Instruction
SLC 5/02 Series B	All types①	1930 µs	1580 µs plus 670 µs per word
SLC 5/02 Series C	All types①	1157 µs	950 µs plus 400 µs per word
SLC 5/03 (All Series)	XIC or XIO	782 µs	—
	OTU, OTE, or OTL	925 µs	—
	COP to M file	—	772 µs plus 23 µs per word
	COP from M file	—	760 µs plus 22 µs per word
	FLL	—	753 µs plus 30 µs per word
	MVM to M file	894 µs	—
	any source or Destination M file address	730 µs	—
SLC 5/04 (All Series)	XIC or XIO	743 µs	—
	OTU, OTE, or OTL	879 µs	—
	COP to M file	—	735 µs plus 23 µs per word
	COP from M file	—	722 µs plus 22 µs per word
	FLL	—	716 µs plus 30 µs per word
	MVM to M file	850 µs	—
	any source or Destination M file address	694 µs	—

① Except the OSR instruction and the instruction parameters noted on page B–3.

SLC 5/02 Processor Example

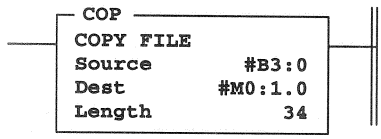


If you are using a SLC 5/02 Series B processor, add 1930 µs to the program scan time for each bit instruction addressed to an M0 or M1 data file. If you are using a SLC 5/02 Series C processor, add 1157 µs.



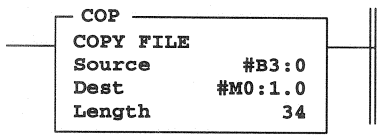
If you are using a SLC 5/02 Series B processor, add 1580 µs plus 670 µs per word of data addressed to the M0 or M1 file. As shown above, 34 words are copied from #B3:0 to M0:1.0. Therefore, this adds 24360 µs to the scan time of the COP instruction. If you are using a SLC 5/02 Series C processor, add 950 µs plus 400 µs per word. This adds 14550 µs to the scan time of the COP instruction.

SLC 5/03 Processor Example



The SLC 5/03 access times depend on the instruction type. Consult the table above for the correct access times to add. As an example, if you use a COP to M file instruction like the one shown above, add 772 µs plus 23 µs per word. This adds 1554 µs to the SLC 5/03 scan time due to the COP instruction.

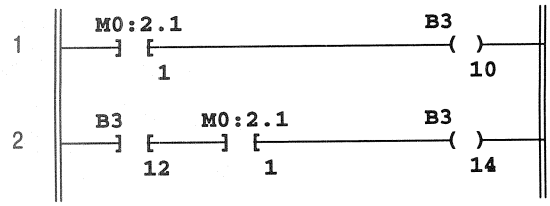
SLC 5/04 Processor Example



The SLC 5/04 access times depend on the instruction type. Consult the table above for the correct access times to add. As an example, if you use a COP to M file instruction like the one shown above, add 735 µs plus 23 µs per word. This adds 1517 µs to the SLC 5/04 scan time due to the COP instruction.

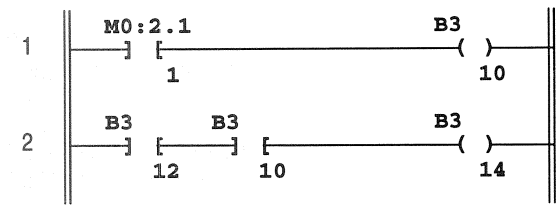
Minimizing the Scan Time

You can keep the processor scan time to a minimum by economizing on the use of instructions addressing the M0 or M1 files. For example, XIC instruction M0:2.1/1 is used in rungs 1 and 2 of the figure below, adding approximately 2 ms to the scan time if you are using a SLC 5/02 Series B processor.



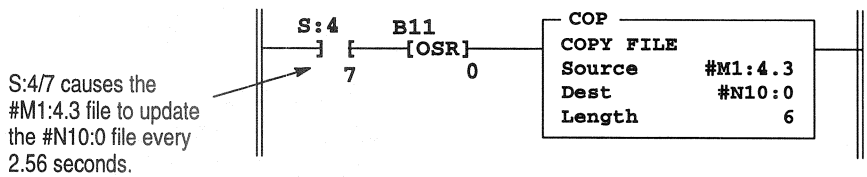
XIC instructions in rungs 1 and 2 are addressed to the M0 data file. Each of these instructions adds approximately 1 ms to the scan time (SLC 5/02 Series B processor).

In the equivalent rungs of the figure below, XIC instruction M0:2.1/1 is used only in rung 1, reducing the SLC 5/02 scan time by approximately 1 ms.



These rungs provide equivalent operation to those of figure A by substituting XIC instruction B3/10 for XIC instruction M0:2.1/1 in rung 2. Scan time is reduced by approximately 1 ms (SLC 5/02 Series B processor).

The following figure illustrates another economizing technique. The COP instruction addresses an M1 file, adding approximately 4.29 ms to the scan time if you are using a SLC 5/02 Series B processor. Scan time economy is realized by making this rung true only periodically, as determined by clock bit S:4/8. (Clock bits are discussed in appendix B of the *SLC 500™ and MicroLogix™ 1000 Instruction Set Reference Manual*, Publication 1747-6.15.) A rung such as this might be used when you want to monitor the contents of the M1 file, but monitoring need not be on a continuous basis.



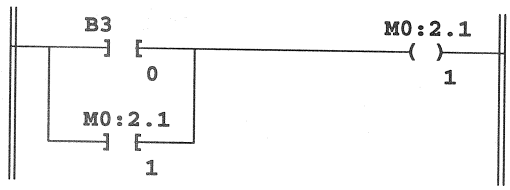
Capturing M0–M1 File Data

The first two ladder diagrams in the last section illustrate a technique allowing you to capture and use M0 or M1 data as it exists at a particular time. In the first figure, bit M0:2.1/1 could change state between rungs 1 and 2. This could interfere with the logic applied in rung 2. The second figure avoids the problem. If rung 1 is true, bit B3/10 captures this information and places it in rung 2.

In the second example of the last section, a COP instruction is used to monitor the contents of an M1 file. When the instruction goes true, the 6 words of data in file #M1:4.3 is captured as it exists at that time and placed in file #N10.0.

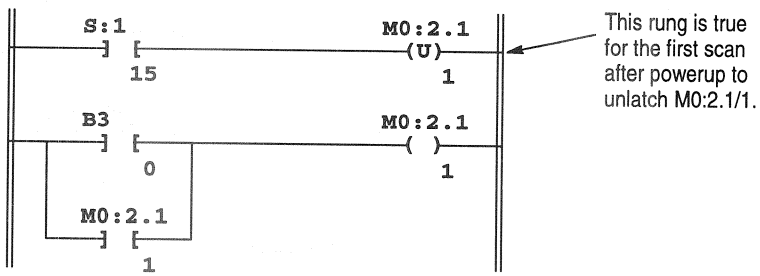
Specialty I/O Modules with Retentive Memory

Certain specialty I/O modules retain the status of M0-M1 data after power is removed. See your specialty I/O module user's manual. This means that an OTE instruction having an M0 or M1 address remains on if it is on when power is removed. A "hold-in" rung as shown below will not function as it would if the OTE instruction were non-retentive on power loss. If the rung is true at the time power is removed, the OTE instruction latches instead of dropping out; when power is again applied, the rung will be evaluated as true instead of false.



ATTENTION: When used with a speciality I/O module having retentive outputs, this rung can cause unexpected start-up on powerup

You can achieve non-retentive operation by unlatching the retentive output with the first pass bit at powerup:



G Files

Some specialty I/O modules use G (confiGuration) files (indicated in the specific specialty I/O module user manual). These files can be thought of as the software equivalent of DIP switches.

The content of G files is accessed and edited offline under the I/O Configuration function. You cannot access G files under the Monitor File function. Data you enter into the G file is passed on to the specialty I/O module when you download the processor file and enter the REM Run or any one of the REM Test modes.

Configuring G Files Using APS Software

The G file is configured as part of the I/O configuration procedure for the processor file. After you have assigned the specialty I/O module to a slot (the procedure is the same as assigning other modules except that you must specify the ID code of the specialty I/O module), the following functions appear at the bottom of the APS screen:

READ CONFIG	ONLINE CONFIG		MODIFY RACKS	MODIFY SLOT	DELETE SLOT	UNDEL SLOT	EXIT	SPIO CONFIG
F1	F2		F4	F5	F6	F7	F8	F9

This is the starting point for configuring the G file and other parameters of the specialty I/O module. Complete the following steps to create and monitor the G file:

1. Press [F9], Specialty I/O Configuration. A screen similar to the following is displayed:

```
I/O CONFIGURATION FOR:EXAMPLE
RACK 1    =      1746-A4  4-SLOT Backplane
RACK 2    =
RACK 3    =
      SLOT      SPECIAL CONFIG FOR SLOT:          1
       *0        Module's ID Code:              12705
       *1        Maximum Input Words:               0
       *2        Maximum Output Words:              0
       *3        Scanned Input Words:               0
        4        Scanned Output Words:              0
        5        M0 Length:                         0
        6        M1 Length:                         0
        7        'G' File Size:                     0
        8        ISR Number:                        0
                 ESC exits
ESC exits

Press a function key
```

ISR NUMBER		MODIFY G FILE		ADVNCD SETUP		G FILE SIZE
F1		F3		F5		F7

2. Press [F7], G File Size, then specify the number of words required for the specialty I/O module.

3. Press [F3], Modify G File. The content of the G file appears in the display area. Data is shown in the default form, decimal:

address	0	1	2	3	4	5	6	7	8	9
G1:0	xxxx	0	0	0	0	0	0	0	0	0
G1:10	0	0	0	0	0	0				

The function keys appearing below the data table indicate the three data formats available to you – binary data, decimal data, and hex/bcd data:

BINARY DATA	DECIMAL DATA	HEX/BCD DATA
F1	F2	F3

The following figure illustrates the three G file data formats that you can select. Word addresses begin with the file identifier G and the slot number you have assigned to the specialty I/O module. In this case, the slot number is 1. Sixteen words have been created (addresses G1:0 through G1:15).

16-word G file, I/O slot 1, decimal format

address	0	1	2	3	4	5	6	7	8	9
G1:0	xxxx	0	0	0	0	0	0	0	0	0
G1:10	0	0	0	0	0	0				

16-word G file, I/O slot 1, hex/bcd format

address	0	1	2	3	4	5	6	7	8	9
G1:0	xxxx	0000	0000	0000	0000	0000	0000	0000	0000	0000
G1:10	0000	0000	0000	0000	0000	0000				

16-word G file, I/O slot 1, binary format

address	15	data		0
G1:0	xxxx	xxxx	xxxx	xxxx
G1:1	0000	0000	0000	0000
G1:2	0000	0000	0000	0000
G1:3	0000	0000	0000	0000
G1:4	0000	0000	0000	0000
G1:5	0000	0000	0000	0000
G1:6	0000	0000	0000	0000
G1:7	0000	0000	0000	0000
G1:8	0000	0000	0000	0000
G1:9	0000	0000	0000	0000
G1:10	0000	0000	0000	0000
G1:11	0000	0000	0000	0000
G1:12	0000	0000	0000	0000
G1:13	0000	0000	0000	0000
G1:14	0000	0000	0000	0000
G1:15	0000	0000	0000	0000

Editing G File Data

Data in the G file must be edited according to your application and the requirements of the specialty I/O module. You edit the data offline under the I/O configuration function only. With the decimal and hex/bcd formats, you edit data at the word level:

- G1:1 = 234 (decimal format)
  G1:1 = 00EA (hex/bcd format)

With the binary format, you edit data at the bit level:

- G1/19 = 1

Important: Word 0 of the G file is configured automatically by the processor according to the particular specialty I/O module. Word 0 cannot be edited.

Interrupt Operation

The I/O event-driven interrupt function is used with SLC 5/02, SLC 5/03, and SLC 5/04 processors. This function allows a specialty I/O module to interrupt the normal processor operating cycle in order to scan a specified subroutine file. Interrupt operation for a specific module is described in the user's manual for the module. You cannot use a standard discrete I/O module to accomplish an I/O event-driven interrupt.

Basic Programming Procedure for the I/O Interrupt Function

- Specialty I/O modules that create interrupts should be configured in the lowest numbered I/O slots. When you are configuring the specialty I/O module slot with the programming device, select the "SPIO CONFIG" function key and program the "ISR" (interrupt subroutine) program file number (range 3 to 255) that you want the SLC processor to execute when the module generates an interrupt.

  Configuring I/O is discussed in chapter 5 in the *Advanced Programming Software User Manual*, Publication 9399-APSUM.
- Create the subroutine file that you have specified as the ISR number.

  Creating a subroutine file is discussed in chapter 6 in the *Advanced Programming Software User Manual*, Publication 9399-APSUM.

Operation

When you restore your program and enter the REM run mode, the I/O interrupt begins operation as follows:

1. The specialty I/O module determines that it needs servicing and generates an interrupt request to the SLC processor.
2. The processor is interrupted from what it is doing, and the specified interrupt subroutine file (ISR) is scanned.
3. When the ISR scan is completed, the specialty I/O module is notified. This informs the specialty I/O module that it is allowed to generate a new interrupt.
4. The processor resumes normal operation from where it left off.

Interrupt Subroutine (ISR) Content

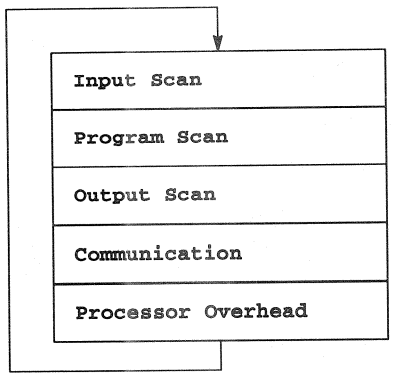
The Interrupt Subroutine (INT) instruction should be the first instruction in your ISR. This identifies the subroutine file as an I/O interrupt subroutine.

The ISR contains the rungs of your application logic. You can program any instruction inside an ISR except a TND, REF, or SVC instruction. IIM or IOM instructions are needed in an ISR if your application requires immediate update of input or output points. Terminate the ISR with an RET (return) instruction.

JSR stack depth is limited to 3. That is, you may call other subroutines to a level 3 deep from an ISR.

Interrupt Latency and Interrupt Occurrences

Interrupt latency is the interval between the I/O module's request for service and the start of the interrupt subroutine. I/O interrupts can occur at any point in your program, but not necessarily at the same point on successive interrupts. Interrupts can only occur between instructions in your program, inside the I/O scan (between slots), or between the servicing of communication packets. The following table shows the interaction between an interrupt and the processor operating cycle.



Events in the processor operating cycle

SLC 5/02 I/O Interrupts	SLC 5/03 and SLC 5/04 I/O Interrupts with Bit S:33/8 set	SLC 5/03 and SLC 5/04 I/O Interrupts with Bit S:33/8 cleared
Between slot updates	Between word updates	Between slot updates
Between instruction updates	Between word updates	Between rung updates
Between slot updates	Between word updates	Between slot updates
Between communication packets	Between word packet updates	Between communication packets
At start and end	Between word updates	Between word updates

Note that ISR execution time adds directly to the overall scan time. During the latency period, the processor is performing operations that cannot be disturbed by the STI interrupt function. Latency periods are:

- SLC 5/02 series B processor interrupts are serviced within 3.7 ms maximum.
- SLC 5/02 series C processor and later interrupts are serviced within 2.4 ms maximum.
- SLC 5/03 and SLC 5/04 processors – If an interrupt occurs while the processor is performing a multi-word slot update and your interrupt subroutine accesses that same slot, the multi-word transfer finishes to completion prior to performing the interrupt subroutine slot access. The SLC Interrupt Latency Bit (S:33/8) functions as follows:
  - When the bit is set (1) interrupts are serviced within 500 µs①.
  - When S:33/8 is clear (0), user interrupts occur between rungs and I/O slot updates.
  - The default state is cleared (0). To determine the interrupt latency with S:33/8 clear, you must calculate the execution time of each and every rung in your program.①

① Interrupt latency varies depending on the processor configuration. See appendix C in the *SLC 500™ and MicroLogix™ 1000 Instruction Set Reference Manual*, Publication 1747-6.15 for more information on how to calculate the interrupt latency.

Interrupt Priorities

Interrupt priorities are as follows:

SLC 5/02 Processor	SLC 5/03 and SLC 5/04 Processors
1. Fault Routine	1. Fault routine
2. STI Subroutine	2. Discrete Input Interrupt (DII)
3. I/O Interrupt Subroutine (ISR)	3. STI Subroutine
	4. I/O Interrupt Subroutine (ISR)

An executing interrupt can only be interrupted by an interrupt having higher priority.

The I/O interrupt cannot interrupt an executing fault routine, an executing DII subroutine, an executing STI subroutine, or another executing I/O interrupt subroutine. If an I/O interrupt occurs while the fault routine, DII, or STI subroutine is executing, the processor waits until the higher priority interrupts are scanned to completion. The I/O interrupt subroutine is then scanned.

Important: *SLC 5/02 specific* – It is important to understand that the I/O Pending bit associated with the interrupting slot remains *clear* during the time that the processor is waiting for the fault routine or STI subroutine to finish.

Important: *SLC 5/03 and SLC 5/04 specific* – The I/O pending bit is always set when the interrupt occurs. You can examine the state of these bits within your higher priority interrupt routines.

If a major fault occurs while executing the I/O interrupt subroutine, execution immediately switches to the fault routine. If the fault was recovered by the fault routine, execution resumes at the point that it left off in the I/O interrupt subroutine. Otherwise, the fault mode is entered.

If a DII interrupt occurs while executing the I/O interrupt subroutine, execution immediately switches to the DII subroutine. When the DII subroutine is scanned to completion, execution resumes at the point that it left off in the I/O interrupt subroutine.

If the STI timer expires while executing the I/O interrupt subroutine, execution will immediately switch to the STI subroutine. When the STI subroutine is scanned to completion, execution resumes at the point that it left off in the I/O interrupt subroutine.

If two or more I/O interrupt requests are detected by the processor at the same instant, or while waiting for a higher or equal priority interrupt subroutine to finish, the interrupt subroutine associated with the specialty I/O module in the lowest slot number is scanned first. For example, if slot 2 (ISR 20) and slot 3 (ISR 11) request interrupt service at the same instant, the processor first scans ISR 20 to completion, then ISR 11 to completion.

Status File Data Saved

Data in the following words is saved on entry to the I/O interrupt subroutine and re-written upon exiting the I/O interrupt subroutine.

- S:0 Arithmetic flags
- S:13 and S:14 Math register
- S:24 Index register

I/O Event Interrupt Parameters

The I/O interrupt parameters below have status file addresses.

- **ISR Number** – Specifies the subroutine file number that will be executed when an I/O interrupt is generated by an I/O module. The ISR Numbers are not part of the status file, but they are part of the I/O configuration for each slot in the SLC system.
- **S:11 and S:12 I/O Slot Enables** – Read/Write. These words are bit mapped to the 30 I/O slots. Bits S:11/1 through S:12/14 refer to slots 1 through 30. Bits S:11/0 and S:12/15 are reserved.

  The enable bit associated with an interrupting slot must be set when an interrupt occurs. Otherwise a major fault will occur. Changes made to these bits using the Data Monitor function take effect at the next end of scan.
- **S:25 and S:26 I/O Interrupt Pending Bits** – Read only. These words are bit mapped to the 30 I/O slots. Bits S:25/1 through S:26/14 refer to slots 1 through 30. Bits S:25/0 and S:26/15 are reserved. The pending bit associated with an interrupting slot is set when the corresponding I/O slot interrupt enable bit is clear at the time of an interrupt request. It is cleared when the corresponding I/O event interrupt enable bit is set, or when an associated RPI instruction is executed. The pending bit for an executing I/O interrupt subroutine remains clear when the ISR is interrupted by a DII, STI, or fault routine.

  SLC 5/02 specific – Likewise, the pending bit remains clear if interrupt service is requested at the time that a higher or equal priority interrupt is executing (fault routine, STI, or other ISR).

SLC 5/03 and SLC 5/04 specific – This bit is set if interrupt service is requested at the time a higher or equal priority interrupt is executing (fault routine, DII, STI, or other ISR).

- **S:27 and S:28 I/O Interrupt Enables** – Read/Write. These words are bit mapped to the 30 I/O slots. Bits S:27/1 through S:28/14 refer to slots 1 through 30. Bits S:27/0 and S:28/15 are reserved. The enable bit associated with an interrupting slot must be set when the interrupt occurs to allow the corresponding ISR to execute. Otherwise the ISR will not execute and the associated I/O slot interrupt pending bit will be set.

  SLC 5/02 specific – Changes made to these bits using the data monitor function or ladder instruction take effect at the next end of scan.

  SLC 5/03 and SLC 5/04 specific – Changes made to these bits using the data monitor function or ladder instruction take effect immediately.

- **S:32 I/O Interrupt Executing Word** – Read only. This word contains the slot number of the specialty I/O module that generated the currently executing ISR. This value is cleared upon completion of the ISR, run mode entry, or upon power up. You can interrogate this word inside of your DII or STI subroutine or fault routine if you wish to know if these higher priority interrupts have interrupted an executing ISR. You may also use this value to discern interrupt slot identity when multiplexing two or more specialty I/O module interrupts to the same ISR.

Status File Display

You can enter and monitor parameters at the status file displays of APS software.

Status File for SLC 5/02 Processors (Display 1)

```
ARITHMETIC FLAGS     S:0            Z:0                    V:0    C:0

PROCESSOR STATUS      00000000 00000000     SUSPEND CODE                  0
PROCESSOR STATUS      00000000 00000001     SUSPEND FILE                  0
PROCESSOR STATUS      00000000 00000000
                                            WATCHDOG      [x10 ms]        10
MINOR FAULT           00000000 00000000     LAST SCAN     [x10 ms]        0
FAULT CODE                      0000        FREE RUNNING CLOCK  00000000 00000000
FAULT DESCRIPTION:

MATH REGISTER                 0000 0000

ACTIVE NODE LIST                            I/O SLOT ENABLES
0         10          20         30         0         10         20         30
0000000 00000000 00000000 0000000           11111111 11111111 11111111 11111111

PROCESSOR BAUD RATE             19200       PROCESSOR ADDRESS             1


Press function key or enter value, press Alt-H for help.
S:0/0 =
offline      no forces                  formatted    decimal addr        File EXAMPLE
```

PAGE UP	PAGE DOWN		SPECIFY ADDRESS		NEXT FILE	PREV FILE	CLR MIN FAULT	CLR MAJ FAULT
F1	F2		F5		F7	F8	F9	F10

Status File for SLC 5/03 Processors (Display 1)

```
ARITHMETIC FLAGS     S:0            Z:0          V:0      C:0

PROCESSOR STATUS      00000000 00000000     SUSPEND CODE              0
PROCESSOR STATUS      00000000 00000001     SUSPEND FILE              0
PROCESSOR STATUS      00000000 00000000
                                            WATCHDOG              [x10 ms] 10
MINOR FAULT           00000000 00000000     LAST SCAN             [x10 ms]  0
FAULT CODE                      0000        FREE RUNNING CLOCK  00000000 11110010
FAULT DESCRIPTION:

MATH REGISTER                 0000 0000

ACTIVE NODE LIST (CHANNEL 1)                I/O SLOT ENABLES
0         10          20         30         0         10         20         30
11000000 00000000 00000000 00000000         11111111 11111111 11111111 11111111

PROCESSOR BAUD RATE (CHANNEL 1) 19200       PROCESSOR ADDRESS (CHANNEL 1)     1


Press a key or enter value, press Alt-H for help.
S:0/0 =
offline      no forces                  formatted    decimal addr        File EXAMPLE
```

PAGE UP	PAGE DOWN		SPECIFY ADDRESS		NEXT FILE	PREV FILE	CLR MIN FAULT	CLR MAJ FAULT
F1	F2		F5		F7	F8	F9	F10

Status File for SLC 5/04 OS400 Processors (Display 1)

```
ARITHMETIC FLAGS    S:0          Z:0                  V:0   C:0

PROCESSOR STATUS     00000000 00000000    SUSPEND CODE                    0
PROCESSOR STATUS     00000000 00000001    SUSPEND FILE                    0
PROCESSOR STATUS     00000000 00000000
                                          WATCHDOG     [x10 ms]           10
MINOR FAULT          00000000 00000000    LAST SCAN    [x10 ms]           0
FAULT CODE                    0000        FREE RUNNING CLOCK  00000000 00000000
FAULT DESCRIPTION:

MATH REGISTER                 0000 0000

                                          I/O SLOT ENABLES
                                          0         10        20        30
                                          11111111 11111111 11111111 11111111


Press function key or enter value, press Alt-H for help.
S:0/0 =
offline      no forces                    formatted    decimal addr        File 09TEST
```

PAGE UP	PAGE DOWN		SPECIFY ADDRESS		NEXT FILE	PREV FILE	CLR MIN FAULT	CLR MAJ FAULT
F1	F2		F5		F7	F8	F9	F10

Status File for SLC 5/04 OS401 Processors (Display 1)

```
ARITHMETIC FLAGS    S:0          Z:0                  V:0   C:0

PROCESSOR STATUS     00000000 00000000    SUSPEND CODE                    0
PROCESSOR STATUS     00000000 00000001    SUSPEND FILE                    0
PROCESSOR STATUS     00000000 00000000
                                          WATCHDOG     [x10 ms]           10
MINOR FAULT          00000000 00000000    LAST SCAN    [x10 ms]           0
FAULT CODE                    0000        FREE RUNNING CLOCK  00000000 00000000
FAULT DESCRIPTION:

MATH REGISTER                 0000 0000

GLOBAL STATUS TRANSMIT WORD             0   I/O SLOT ENABLES
GLOBAL STATUS WORD TRANSMIT ENABLE      0   0         10        20        30
GLOBAL STATUS WORD RECEIVE ENABLE       0   11111111 11111111 11111111 11111111

PROCESSOR BAUD RATE (CHANNEL 1)   57600     PROCESSOR ADDRESS   01 octal (01 dec)

Press function key or enter value, press Alt-H for help.
S:0/0 =
offline      no forces                    formatted    decimal addr        File EXAMPLE
```

PAGE UP	PAGE DOWN		GLOBAL STATUS	SPECIFY ADDRESS		NEXT FILE	PREV FILE	CLR MIN FAULT	CLR MAJ FAULT
F1	F2		F4	F5		F7	F8	F9	F10

Status File for SLC 5/02 Processors (Display 2)

```
                                        I/O SLOT INTERRUPT ENABLES
LAST SCAN [x10 ms]:              0      0         10         20         30
                                        00000000 00000000 00000000 00000000
AVERAGE SCAN [x10 ms]:           0
MAXIMUM SCAN [x10 ms]:           1      I/O SLOT INTERRUPT PENDING
                                        0         10         20         30
INDEX REGISTER VALUE:            4      00000000 00000000 00000000 00000000
INDEX ACROSS FILES:              NO

FAULT ROUTINE SUBROUTINE FILE:   0      I/O INTERRUPT FILE EXEC:          0

SELECTABLE TIMED INTERRUPT              SINGLE STEP TEST          FILE  RUNG
 SUBROUTINE FILE:                0       START STEP ON:             2     3
 SETPOINT [x10 ms]:              0       END STEP BEFORE:           0     0
 ENABLED:                        1       FAULT/POWER DOWN:          2     3
 EXECUTING:                      0       COMPILED FOR SINGLE STEP:        NO
 PENDING:                        0
 1 ms TIMEBASE                   0      STI LOST:                         0

Press a key or enter value, press Alt-H for help.
S:28/15 =
offline      no forces                    formatted    decimal addr          File EXAMPLE
```

PAGE UP (F1) PAGE DOWN (F2) SPECIFY ADDRESS (F5) NEXT FILE (F7) PREV FILE (F8)

Status File for SLC 5/03 and SLC 5/04 Processors (Display 2)

```
LAST SCAN (x01 ms)               0      I/O SLOT INTERRUPT ENABLES
LAST SCAN [x10 ms]:              0      0         10         20         30
1 ms TIMEBASE (SCAN Times)       0      00000000 00000000 00000000 00000000
AVERAGE SCAN [x10 ms]:           0
MAXIMUM SCAN [x10 ms]:           1
                                        I/O SLOT INTERRUPT PENDING
INDEX REGISTER VALUE:            4      0         10         20         30
INDEX ACROSS FILES:              NO     00000000 00000000 00000000 00000000

FAULT ROUTINE SUBROUTINE FILE:   0      I/O INTERRUPT FILE EXEC:          0

SELECTABLE TIMED INTERRUPT              SINGLE STEP TEST          FILE  RUNG
 SUBROUTINE FILE:                0       START STEP ON:             2     3
 SETPOINT [x10 ms]:              0       END STEP BEFORE:           0     0
 ENABLED:                        1       FAULT/POWER DOWN:          2     3
 EXECUTING:                      0       COMPILED FOR SINGLE STEP:      YES
 PENDING:                        0
 1 ms TIMEBASE                   0      STI LOST:                         1
Press a key or enter value, press Alt-H for help.
S:28/15 =
offline      no forces                    formatted    decimal addr          File EXAMPLE
```

PAGE UP (F1) PAGE DOWN (F2) GLOBAL STATUS (F4) ① SPECIFY ADDRESS (F5) NEXT FILE (F7) PREV FILE (F8)

① This function key is only available for SLC 5/04 OS401 processors.

Status File for SLC 5/03 and SLC 5/04 Processors (Display 3)

```
EXT PROCESSOR STATUS    0000000 00000000      REAL TIME CLOCK DATE:      11-17-1995
EXT MINOR FAULT         0000000 00000000                   TIME:         2:15.34

DISCRETE INPUT INTERRUPT
  SUBROUTINE FILE:                  3     MASK:                       00000001
  INPUT SLOT:                       1     COMPARE VALUE:              00000001
  ENABLED                           1     PRESET:                            1
  EXECUTING:                        0     RETURN MASK:                00000000
  PENDING:                          0     ACCUMULATOR:                       0
  OVERFLOW:                         0     LAST SCAN [ms]:                    0
  LOST:                             0     MAX. SCAN [ms]:                    0

PROCESSOR                    OPERATING SYSTEM        USER PROGRAM
  CATALOG #:          0        CATALOG #:     0        FUNCTIONAL TYPE:     0
  SERIES:             0        SERIES:        0        FUNCTIONAL INDEX:    0
  REVISION:           0        F.R.N.:        0
  USER RAM SIZE:      0
  FLASH EEPROM SIZE:  0

Press a key or enter value, press Alt-H for help.
S:37 =
offline      no forces                        formatted    decimal addr        File EXAMPLE
```

PAGE UP	PAGE DOWN	GLOBAL STATUS	SPECIFY ADDRESS	NEXT FILE	PREV FILE
F1	F2	F4 ①	F5	F7	F8

① This function key is only available for SLC 5/04 OS401 processors.

Status File for SLC 5/03 Processors (Display 4)

```
                                        EXT PROCESSOR STATUS: 00000000 00000000
CHANNEL 0 ACTIVE NODE TABLE

            0         10        20        30
    0-31    00000000 00000000 00000000 00000000
   32-63    00000000 00000000 00000000 00000000
   64-95    00000000 00000000 00000000 00000000      10 µs DII TIMER:     0
  96-127    00000000 00000000 00000000 00000000      10 µs STI TIMER:     0
 128-159    00000000 00000000 00000000 00000000      10 µs I/O TIMER:     0
 160-191    00000000 00000000 00000000 00000000
 192-223    00000000 00000000 00000000 00000000
 224-255    00000000 00000000 00000000 00000000

Press a key or enter value, press Alt-H for help.
S:34/0 =
offline      no forces                      formatted    decimal addr        File EXAMPLE
```

PAGE UP	PAGE DOWN	SPECIFY ADDRESS	NEXT FILE	PREV FILE
F1	F2	F5	F7	F8

Status File for SLC 5/04 Processors (Display 4)

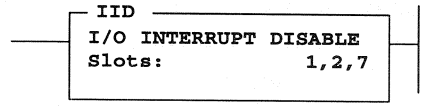
```
                                        EXT PROCESSOR STATUS: 00000000 00000000
CHANNEL 0 ACTIVE NODE TABLE

            0         10        20        30

    0-31    00000000 00000000 00000000 00000000
   32-63    00000000 00000000 00000000 00000000
   64-95    00000000 00000000 00000000 00000000      10 µs DII TIMER:     0
  96-127    00000000 00000000 00000000 00000000      10 µs STI TIMER:     0
 128-159    00000000 00000000 00000000 00000000      10 µs I/O TIMER:     0
 160-191    00000000 00000000 00000000 O0000000
 192-223    00000000 00000000 00000000 00000000
 224-255    00000000 00000000 00000000 00000000

CHANNEL 1 ACTIVE NODE TABLE (octal)

            0        10       20       30
    0-37    00000000 00000000 00000000 00000000
   40-77    00000000 00000000 00000000 00000000


Press a key or enter value, press Alt-H for help.
S:34/0 =
offline      no forces                    formatted    decimal addr         File EXAMPLE
```

PAGE UP	PAGE DOWN	GLOBAL STATUS	SPECIFY ADDRESS	NEXT FILE	PREV FILE
F1	F2	F4 ①	F5	F7	F8

① This function key is only available for SLC 5/04 OS401 processors.

I/O Interrupt Disable (IID) and I/O Interrupt Enable (IIE)

Use the I/O Interrupt Disable (IID) and I/O Interrupt Enable (IIE) instructions to create zones in which I/O interrupts cannot occur.



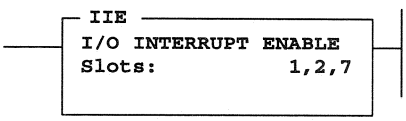
I/O Interrupt Disable – IID

Use this instruction together with an IIE instruction to create a zone in your main ladder program file or subroutine file in which I/O interrupts cannot occur. The IID instruction takes effect immediately upon execution.

SLC 5/02 specific – Setting/clearing the I/O interrupt enable bits (S:27 and S:28) with a programming device or standard instruction such as MVM takes effect at the END of the scan only.

SLC 5/03 and SLC 5/04 specific – Setting/clearing the I/O interrupt enable bits (S:27 and S:28) with a programming device or standard instruction such as MVM takes effect immediately.

When true, this instruction clears the I/O interrupt enable bits (S:27/1 through S:28/14) corresponding to the slots parameter of the instruction (slots 1, 2, 7 in the example above). Interrupt subroutines of the affected slots will not be able to execute when an interrupt request is made. Instead, the corresponding I/O pending bits (S:25/1 through S:26/14) will be set. The ISR will not be executed until an IIE instruction with the same slot parameter is executed, or until the end of the scan during which you use a programming device to set the corresponding status file bit.



I/O Interrupt Enable – IIE

Use this instruction together with the IID instruction to create a zone in your main ladder program file or subroutine file in which I/O interrupts cannot occur. The IIE instruction takes effect immediately upon execution.

SLC 5/02 specific – Setting/clearing the I/O interrupt enable bits (S:27 and S:28) with a programming device or standard instruction such as MVM takes effect at the END of the scan only.

SLC 5/03 and SLC 5/04 specific – Setting/clearing the I/O interrupt enable bits (S:27 and S:28) with a programming device or standard instruction such as MVM takes effect immediately.

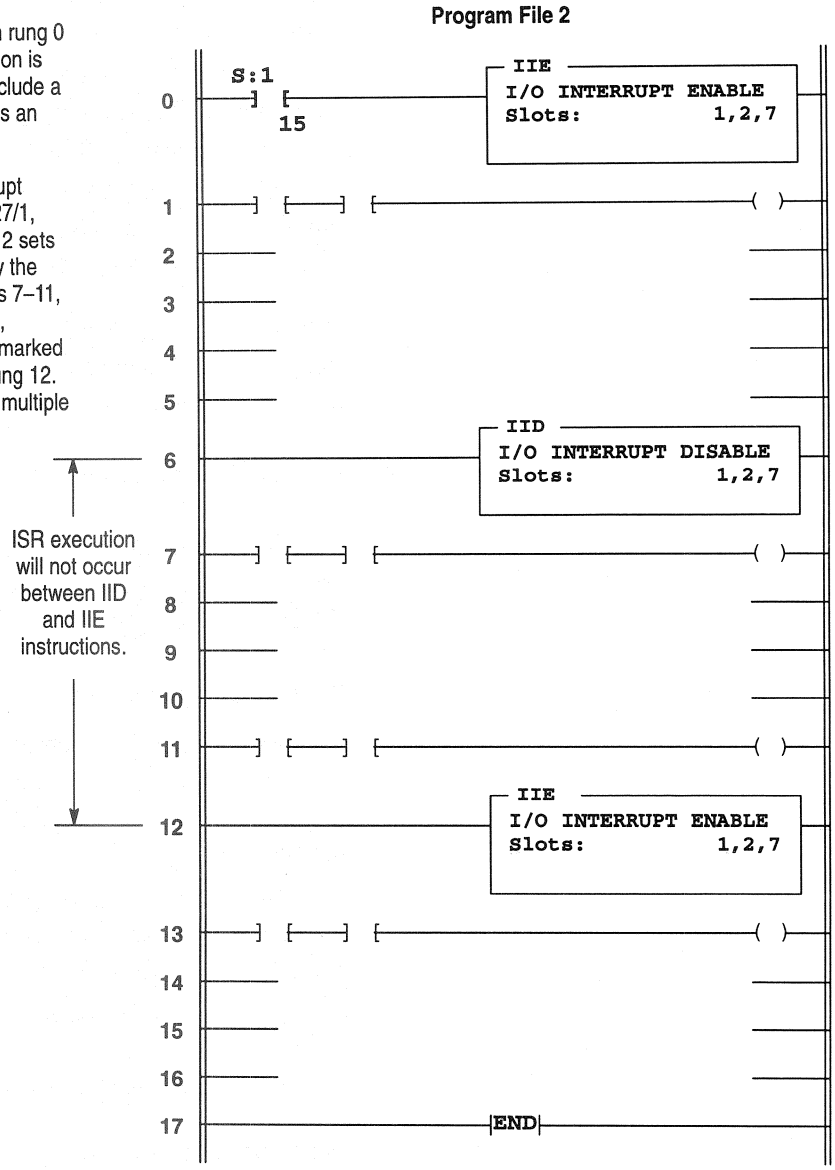
When true, this instruction sets the I/O interrupt enable bits (S:27/1 through S:28/14) corresponding to the slots parameter of the instruction (slots 1, 2, 7 in the example above). Interrupt subroutines of the affected slots will regain the ability to execute when an interrupt request is made. If an interrupt was pending (S:25/1 through S:26/14) and the pending slot corresponds to the IIE slots parameter, the ISR associated with that slot will execute immediately.

IID/IIE Zone Example

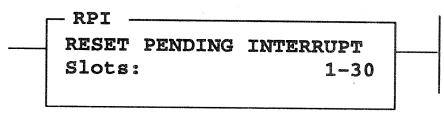
In the program below, slots 1, 2, and 7 are capable of generating I/O interrupts. The IID and IIE instructions in rungs 6 and 12 are included to avoid having I/O interrupt ISRs execute as a result of interrupt requests from slots 1, 2, or 7. This allows rungs 7 through 11 to execute without interruption.

The first pass bit S:1/15 and the IIE instruction in rung 0 are included to insure that the I/O interrupt function is initialized following a power cycle. You should include a rung such as this any time your program contains an IID/IIE zone or an IID instruction.

The IID instruction in rung 6 clears the I/O interrupt enable bits associated with slots 1, 2, and 7 (S:27/1, S:27/2, and S:27/7). The IIE instruction in rung 12 sets these same bits. If an I/O interrupt is detected by the processor while the processor is executing rungs 7–11, the interrupt will be marked as pending. (S:25/1, S:25/2, and/or S:25/7 will be set.) All interrupts marked as pending will be serviced upon execution of rung 12. The lowest numbered slot is serviced first when multiple pending bits are set.



Reset Pending Interrupt (RPI)



The RPI instruction resets the pending status of the specified slots and informs the corresponding I/O modules that you have aborted their interrupt requests. This instruction is not required to configure a basic I/O interrupt application.

When true, this instruction clears the I/O pending bits (S:25/1 through S:26/14) corresponding to the slots parameter of the instruction. In addition, the processor notifies the specialty I/O modules in those slots that their interrupt request was aborted. Following this notice, the slot may once again request interrupt service. This instruction does *not* affect the I/O slot interrupt enable bits (S:27/1 through S:28/14).

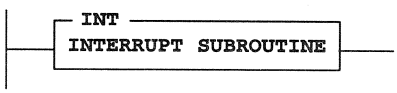
Entering Parameters

Enter the I/O slot numbers (1 to 30) involved.

Examples:

6	indicates slot 6
6,8	indicates slots 6 and 8
6–8	indicates slots 6, 7, and 8
1–30	indicates all slots

Interrupt Subroutine (INT)



Use the INT instruction in I/O event-driven interrupt subroutines (ISRs) and STIs for identification purposes. Use of this instruction is optional.

This instruction has no control bits and is always evaluated as true. When used, the INT should be programmed as the first instruction of the first rung of the ISR.

Differential Encoder Information

This appendix describes the wiring procedures for connecting a differential encoder to the module.

Connecting a Differential Encoder

For proper module operation, wire the encoder so that the Z input signal is high (true) at the same time the A and B input signals are low (false). If this condition is not met, inconsistent homing may occur.

If you are using an Allen–Bradley Bulletin 845H differential encoder, this condition is met by following this manual's wiring diagrams. The following instructions describe how to connect a differential encoder to the module.

1. Obtain the encoder output timing diagram from the encoder data sheets.
2. On the timing diagram, look at the Z input signal and its complement Z signal. Whichever signal is low for most of the encoder revolution and pulses high for the marker interval should be wired into the Z(+) terminal. The remaining signal should be wired into the Z(–) terminal.
3. Look at the B input signal and its complement B signal. Whichever signal is low for at least part of the marker interval should be wired to the B(+) terminal. It is possible that both signals meet this condition. It this is the case, either signal may be wired to the B(+) terminal. The remaining signal should be wired into the B(–) terminal.
4. Look at the A input signal and its complement A signal. Whichever signal is low for at least part of the marker interval should be wired to the A(+) terminal. It is possible that both signals meet this condition. It this is the case, either signal may be wired to the A(+) terminal. The remaining signal should be wired into the A(–) terminal.
5. Since the encoder may be mounted on either end of a motor shaft, the encoder may spin CW or CCW for a given shaft direction. As a result, the direction (phasing) of the encoder may be backwards. If this is the case, switch the Channel A wires with the Channel B wires. This changes the direction of the encoder signals. The wire at A(+) exchanges with wire at B(+). The wire at A(–) exchanges with wire at B(–).

Special Considerations When Using APS Versions 2.01 and 3.01

Read this appendix if you are using APS 1747–PA2E Series C or D, 1747–PA2F Series C, 1747–PA2G, Series C, or 1747–PA2J Series C with the High–Speed Counter module.

ATTENTION: Failure to adhere to these instructions could result in unexpected input and/or output operation.

Nature of the APS Software Problem

APS may calculate I/O addresses that do not correspond to the actual location of the I/O in memory. This happens because APS does not recognize edits made to the specialty I/O (SPIO) configuration for modules that use an extended mix code (that is, when you are prompted to enter the maximum number of input words and maximum number of output words to configure). Currently, the High–Speed Counter module is the only module with such a code.

Preventing the APS Problem from Occurring

To prevent the APS problem from occurring, you must:

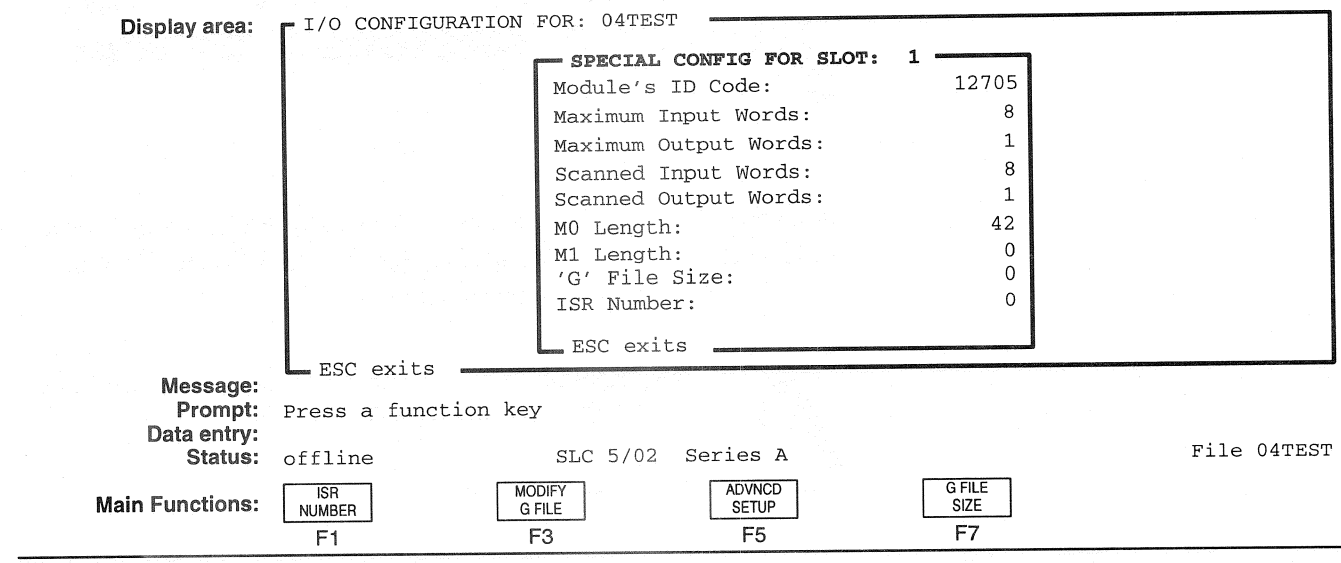
- verify the SPIO configuration of your module
- force APS to resave your I/O configuration
- save and restore your application program

Verifying the SPIO Configuration of Your High–Speed Counter Module

To verify the SPIO configuration of your module, follow these instructions:

1. From the APS main screen, press: OFFLINE PRG/DOC (F3), then PROCSSR FUNCTNS (F1), then CHANGE PROCSSR (F1), then CONFIGR I/O (F5). Select the High–Speed Counter module and press SPIO CONFIG (F9).

The following screen appears:



2. Make sure that the parameters in the SPECIAL CONFIG FOR SLOT display are as follows:

Parameter:	Parameter Value:
Module's ID Code	12705
Maximum Input Words	8
Maximum Output Words	1
Scanned Input Words	8①
Scanned Output Words	1①
M0 Length	42
M1 Length	0
'G' File Size	0
ISR Number	0

① You may change these values per your application needs.

Important: If your High–Speed Counter module has not been previously installed, make sure that you enter the values above correctly. If you do not, your control application for the High–Speed Counter module will not work as expected.

3. Change any values in the SPECIAL CONFIG FOR SLOT display that are incorrect. See the following table for details.

To Change this Parameter:	Press this Function Key:
Module's ID Code	[F5] – ADVNCD SETUP
Maximum Input Words	
Maximum Output Words	
Scanned Input Words	
Scanned Output Words	
M0 Length	
M1 Length	
'G' File Size	[F7] – G FILE SIZE①
ISR Number	[F1] – ISR NUMBER①

① These keys are not applicable to the HSCE module.

4. Return to the previous screen by pressing **[ESC]** twice.

APS displays the following screen:

Display area:

```
I/O CONFIGURATION FOR: 04TEST
RACK 1  =       1746-A4 4-slot Backplane
RACK 2  =       NOT INSTALLED
RACK 3  =       NOT INSTALLED

   SLOT         CATALOG #       CARD DESCRIPTION
   * 0          1747-L524     5/02 CPU-4k USER MEMORY
   * 1          1746-HSCE     HIGH-SPEED COUNTER/ENCODER
   * 2          1746-IA4       4-Input 100/200 VAC
   * 3
     4
     5
     6
     7
     8
ESC exits
```

Message:
Prompt: Press a function key
Data entry:
Status: offline SLC 5/02 Series A File 04TEST

Main Functions:

MODIFY RACKS	MODIFY SLOT	DELETE SLOT	UNDEL SLOT	EXIT	SPIO CONFIG
F4	F5	F6	F7	F8	F9

Forcing APS to Resave Your I/O Configuration

To force APS to resave your I/O configuration, you need to delete *and* immediately undelete one I/O module from its configured slot. (Do not delete and undelete your processor configuration.) Do the following:

1. Select an I/O module to delete and undelete with your up/down cursor keys.
2. Press DELETE SLOT (F6), then YES (F8), then UNDEL SLOT (F7).
3. Save and exit the I/O configuration menu, by pressing EXIT (F8), then SAVE & EXIT (F8).

Saving and Restoring Your Application Program

Once you have completed the previous tasks, you must save your application program. Once your application program is saved, you must restore the program to the processor. To do this, follow the procedures detailed in the *Advanced Programming Software User Manual*.

Range/Rate Mode Configuration Worksheets

Shown on the following page is the Range/Rate Mode Configuration Worksheet for the Output and M0 File.

Output and M0 File Worksheets

ATTENTION: The module will fault on power-up if you do not enter values for the Setup and Control Word, Valid Ranges, Rate Period, and Reset Value/Maximum Count Value.

Direct Outputs (page 4–15)

Bit Number (decimal)	*15*	*14*	*13*	*12*	*11*	*10*	*9*	*8*
Output Number								
Direct Outputs	R	R	R	R	R	R	R	R

7	*6*	*5*	*4*	*3*	*2*	*1*	*0*	
7	6	5	4	3	2	1	0	
								O:e.0

1 = output ON if under processor control

Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

Output Source Select (page 4–5)

Bit Number (decimal)	*15*	*14*	*13*	*12*	*11*	*10*	*9*	*8*
Output Source Select	R	R	R	R	R	R	R	R

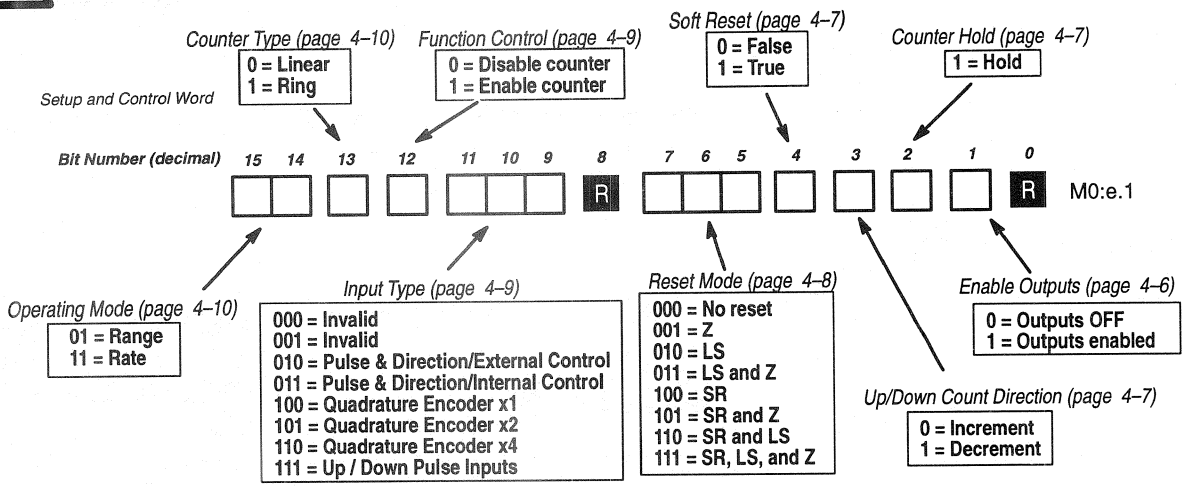
7	*6*	*5*	*4*	*3*	*2*	*1*	*0*	
								M0:e.0

1 = processor 0 = module

Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

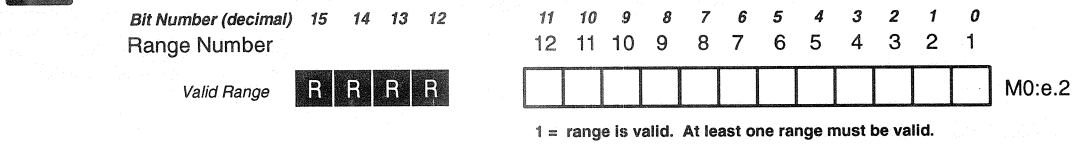
Setup and Control Word (page 4–6)

ATTENTION: The module will fault on power-up if you do not enter a value.

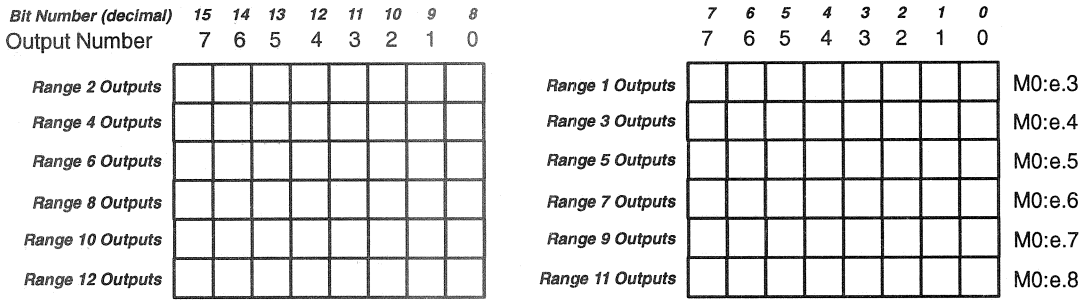


Valid Ranges (page 4–11)

ATTENTION: The module will fault on power-up if you do not enter a value.

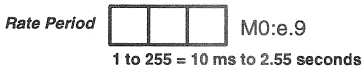


Range Outputs (page 4–11)



Rate Period (decimal) (page 4–12)

ATTENTION: The module will fault on power-up if you do not enter a value.



R = Reserved, must be reset to 0

Starting and Ending Range Values (decimal) (page 4–12)

Range 1 Starting Value		**M0:e.10**
Range 1 Ending Value		M0:e.11
Range 2 Starting Value		**M0:e.12**
Range 2 Ending Value		M0:e.13
Range 3 Starting Value		**M0:e.14**
Range 3 Ending Value		M0:e.15
Range 4 Starting Value		**M0:e.16**
Range 4 Ending Value		M0:e.17
Range 5 Starting Value		**M0:e.18**
Range 5 Ending Value		M0:e.19
Range 6 Starting Value		**M0:e.20**
Range 6 Ending Value		M0:e.21
Range 7 Starting Value		**M0:e.22**
Range 7 Ending Value		M0:e.23
Range 8 Starting Value		**M0:e.24**
Range 8 Ending Value		M0:e25
Range 9 Starting Value		**M0:e.26**
Range 9 Ending Value		M0:e.27
Range 10 Starting Value		**M0:e.28**
Range 10 Ending Value		M0:e.29
Range 11 Starting Value		**M0:e.30**
Range 11 Ending Value		M0:e.31
Range 12 Starting Value		**M0:e.32**
Range 12 Ending Value		M0:e.33

Reset Value/Maximum Count Value (page 4–13)

ATTENTION: The module will fault on power-up if you do not enter a value.

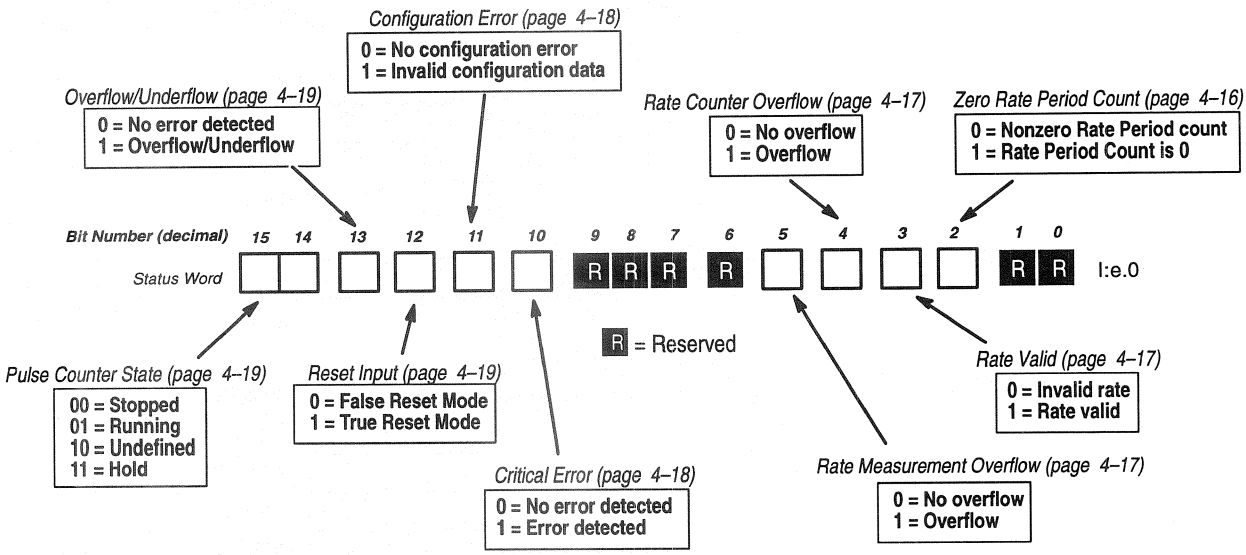
Reset Value/Maximum Count Value | | | | | | M0:e.34

Ring counter – Maximum Count Value range is 1 to 32767 (rollover at +32767)
Linear counter – Reset Value range is –32767 to +32767.

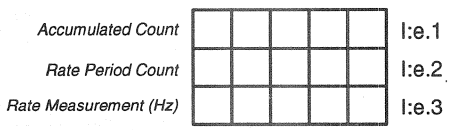
Input Data File Worksheets

Shown below is the Range/Rate Mode Configuration Worksheet for the Input File.

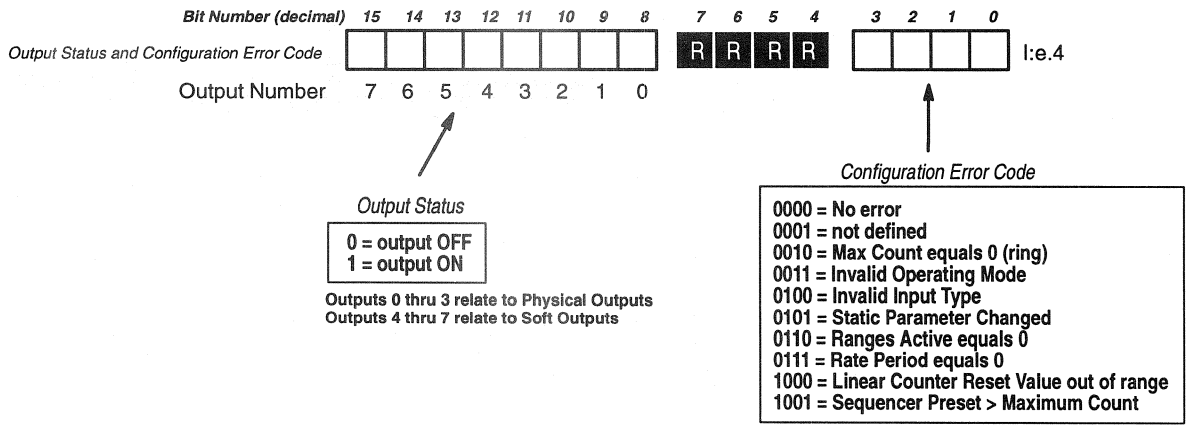
Status Word (page 4–16)



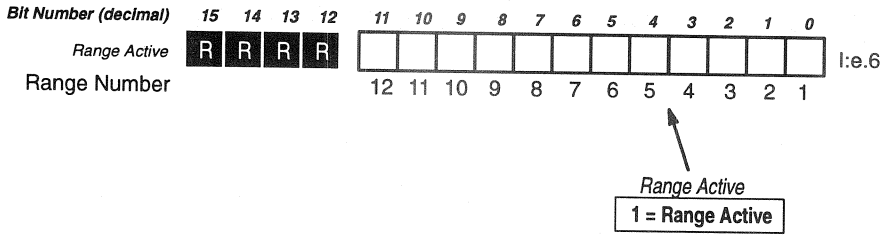
Accumulated Count, Rate Period Count, and Rate Measurement (decimal) (page 4–19)



Output Status and Configuration Error Code (page 4–20)



Range Active (page 4–21)



Module Setup Information (page 4–21)

Module ID Code = 12705 (8 Input and 1 Output word)
42 M0 File words

File size – 42 word integer file, 42 word M0 File

Sequencer Mode Configuration Worksheets

Output and M0 File Worksheets

Shown on the following page is the Sequencer Mode Configuration Worksheet for the Output and M0 File.

ATTENTION: The module will fault on power–up if you do not enter values for the Setup and Control Word, Valid Steps, Rate Period, and Reset Value/Maximum Count Value.

Direct Outputs (page 4–32)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Number								
Direct Outputs	R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0	
								O:e.0

1 = output ON if under processor control
Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

Output Source Select (page 4–22)

Bit Number (decimal)	15	14	13	12	11	10	9	8
Output Source Select	R	R	R	R	R	R	R	R

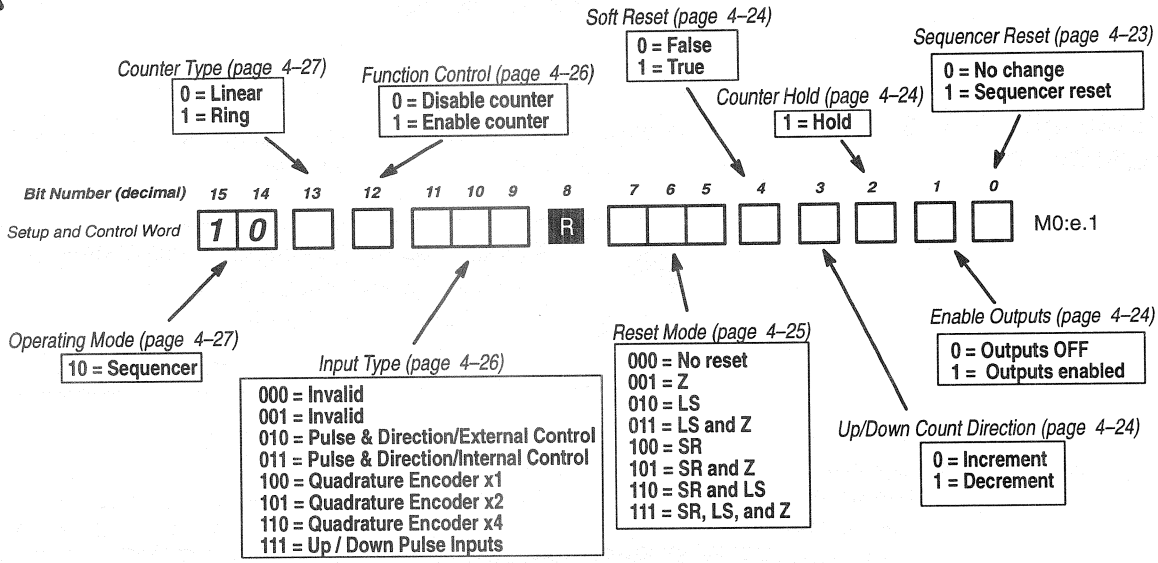
R = Reserved, must be reset to 0

7	6	5	4	3	2	1	0	
								M0:e.0

1 = processor 0 = Module
Bits 0 thru 3 relate to Physical Outputs
Bits 4 thru 7 relate to Soft Outputs

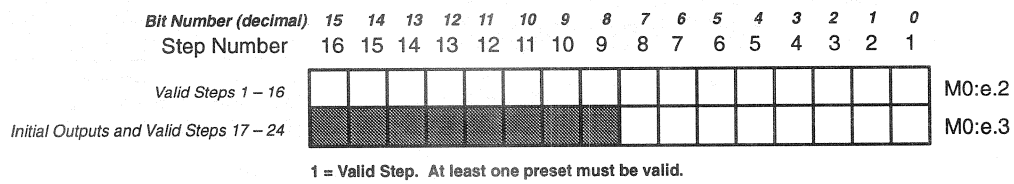
Setup and Control Word (page 4–23)

ATTENTION: The module will fault on power–up if you do not enter a value.



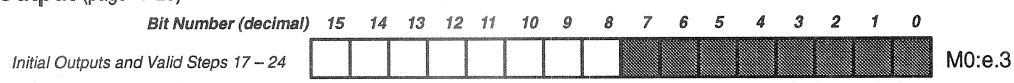
Valid Steps (page 4–28)

ATTENTION: The module will fault on power–up if you do not enter a value.



1 = Valid Step. At least one preset must be valid.

Initial Output (page 4–28)



The Initial Output is the output pattern's starting position

Step Outputs (page 4–29)

Bit Number (decimal)	15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0	
Output Number	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
Step 2 Outputs									*Step 1 Outputs*									**M0:e.4**
Step 4 Outputs									*Step 3 Outputs*									M0:e.5
Step 6 Outputs									*Step 5 Outputs*									**M0:e.6**
Step 8 Outputs									*Step 7 Outputs*									M0:e.7
Step 10 Outputs									*Step 9 Outputs*									**M0:e.8**
Step 12 Outputs									*Step 11 Outputs*									M0:e.9
Step 14 Outputs									*Step 13 Outputs*									**M0:e.10**
Step 16 Outputs									*Step 15 Outputs*									M0:e.11
Step 18 Outputs									*Step 17 Outputs*									**M0:e.12**
Step 20 Outputs									*Step 19 Outputs*									M0:e.13
Step 22 Outputs									*Step 21 Outputs*									**M0:e.14**
Step 24 Outputs									*Step 23 Outputs*									M0:e.15

Rate Period (decimal) (page 4–30)

ATTENTION: The module will fault on power–up if you do not enter a value.

Rate Period [ ][ ][ ] M0:e.16

1 to 255 = 10 ms to 2.55 seconds

Step Preset Values (decimal) (page 4–30)

Step 1 Preset						**M0:e.17**	*Step 13 Preset*						M0:e.29
Step 2 Preset						M0:e.18	*Step 14 Preset*						**M0:e.30**
Step 3 Preset						**M0:e.19**	*Step 15 Preset*						M0:e.31
Step 4 Preset						M0:e.20	*Step 16 Preset*						**M0:e.32**
Step 5 Preset						**M0:e.21**	*Step 17 Preset*						M0:e.33
Step 6 Preset						M0:e.22	*Step 18 Preset*						**M0:e.34**
Step 7 Preset						**M0:e.23**	*Step 19 Preset*						M0:e.35
Step 8 Preset						M0:e.24	*Step 20 Preset*						**M0:e.36**
Step 9 Preset						**M0:e.25**	*Step 21 Preset*						M0:e.37
Step 10 Preset						M0:e.26	*Step 22 Preset*						**M0:e.38**
Step 11 Preset						**M0:e.27**	*Step 23 Preset*						M0:e.39
Step 12 Preset						M0:e.28	*Step 24 Preset*						**M0:e.40**

Reset Value/Maximum Count Value (page 4–31)

ATTENTION: The module will fault on power–up if you do not enter a value.

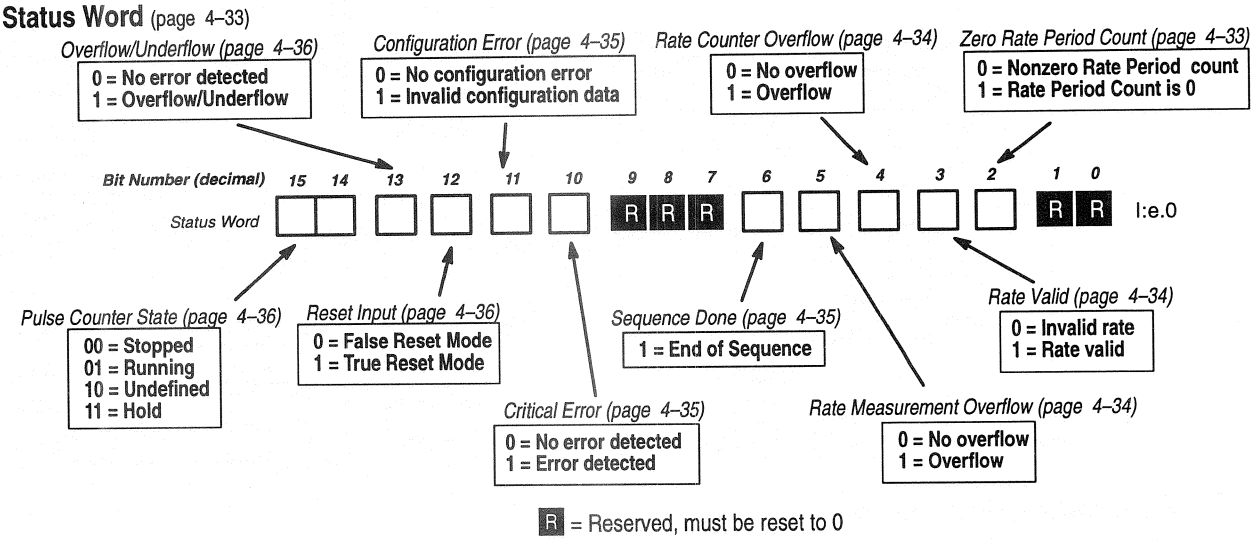
Reset Value/Maximum Count Value [ ][ ][ ][ ][ ] M0:e.41

Ring counter – Maximum Count Value range is 1 to 32767 (rollover at +32767)
Linear counter – Reset Value range is –32767 to +32767.

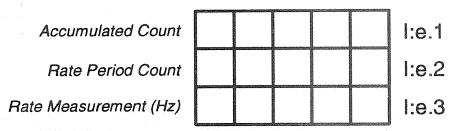
Input Data File Worksheets

Shown below is the Sequencer Mode Configuration Worksheet for the Input Data file.

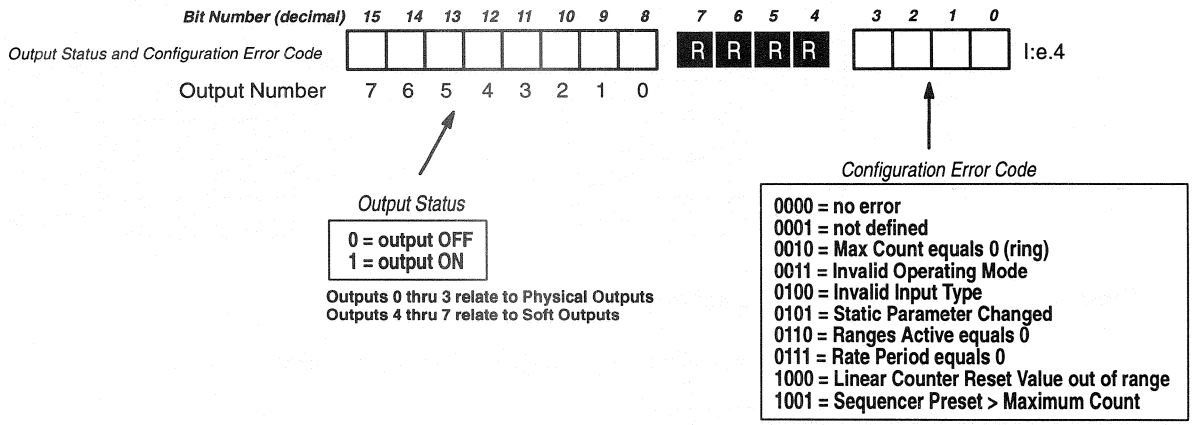
Status Word (page 4–33)



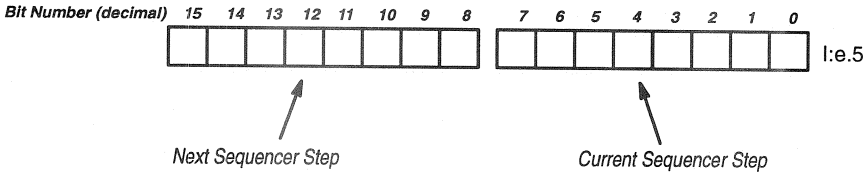
Accumulated Count, Rate Period Count, and Rate Measurement (decimal) (page 4–36)



Output Status and Configuration Error Code (page 4–37)



Next Sequencer Step and Current Sequencer Step (page 4–38)



Next Sequencer Step Preset (decimal) (page 4–38)

Module Setup Information

Module ID Code = 12705 (8 Input and 1 Output word)
File Size – 42 word integer file, and 42 word M0 File

Glossary

The following terms and abbreviations are specific to this product. For a complete listing of Allen–Bradley terminology, refer to the *Allen–Bradley Industrial Automation Glossary*, Publication Number AG–7.1.

Input File — Refers to the module's Input Data File. This file is updated during the SLC processor input scan.

Output File — Refers to the module's Output Data File. This file is updated during the SLC processor output scan.

M Files — Refers to the M0 module data files that reside in the module. M files contain setup and control information. The contents of these files can be accessed by your user program.

Module — Refers to the High–Speed Counter Module, Catalog Number 1746–HSCE.

Physical Outputs — Refers to actual outputs on the module.

Soft Outputs — Refers to status bits within the module that can be seen by the module's program and examined by your user program.

SLC Processor — Refers to the 5/02 (or later) SLC processor that controls the SLC chassis where the module is located.

Dynamic Parameter — Refers to a configuration parameter that can be altered while the counter is operating.

Static Parameter — Refers to a parameter that must not be altered while the counter is operating.

Critical Error — Refers to an error that halts module operation and turns module controlled outputs OFF.

A

B

C

D

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F

G

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L

M

N

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P

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Z

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